

Petra UMA Schematics Document Ivy Bridge Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

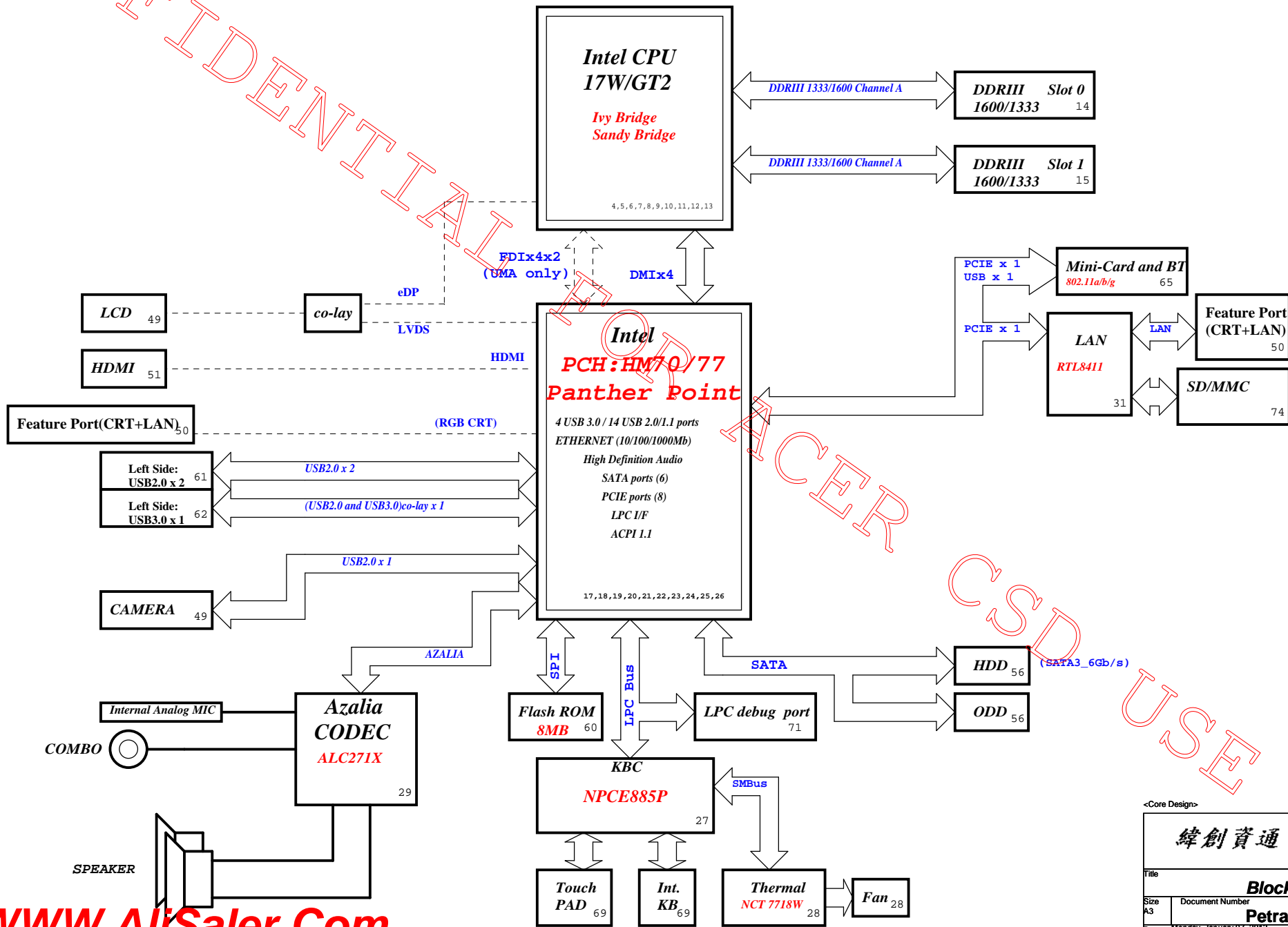
Petra Uma

Date: Wednesday, February 22, 2012

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Rev
-1

Project code : 91.4VM01.001
PCB P/N : 48.4VM02.001
PCB No. : 11324
Revision : -1



CHARGER	
BQ24727 40	
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
RT8223MGQW 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
CPU DC/DC	
ISL95836HRTZ 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
ISL95836HRTZ 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
SYSTEM DC/DC	
TPS51218DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
RT8207LGQW 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
LDO	
RT9025-25ZSP 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0
LDO	
G978 48	
INPUTS	OUTPUTS
1D05V_VTT	0D85V_S0
PCB LAYER	
L1:Top L4:Signal L2:VCC L5:GND L3:Signal L6:Bottom	

<Core Design>

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21E, 28, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram

Size: A3 Document Number: Petra Uma Rev: -1

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PCB Strapping Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor / CRB has it pulled up with 1-kohm no-stuff resistor. Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

Processor Strapping Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
		ACTIVE IN	
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_SFPCORE 1D8V_VGA_S0 1D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 3.3V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	5V-14.1V 5V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses	Ref Des	HURON RIVER ORB
Device	Address	Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

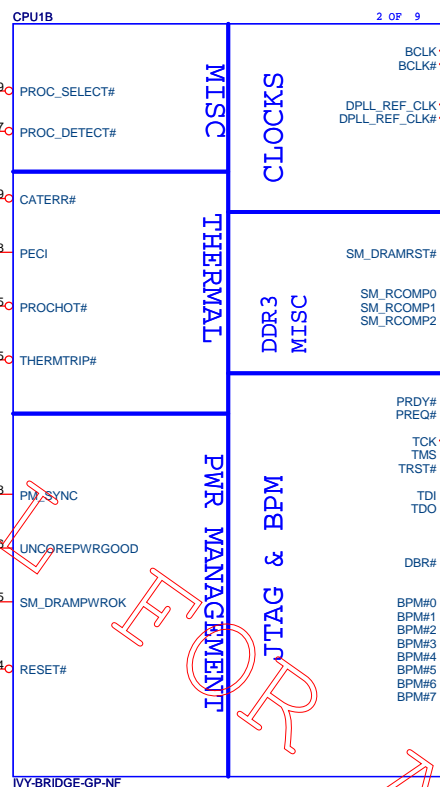
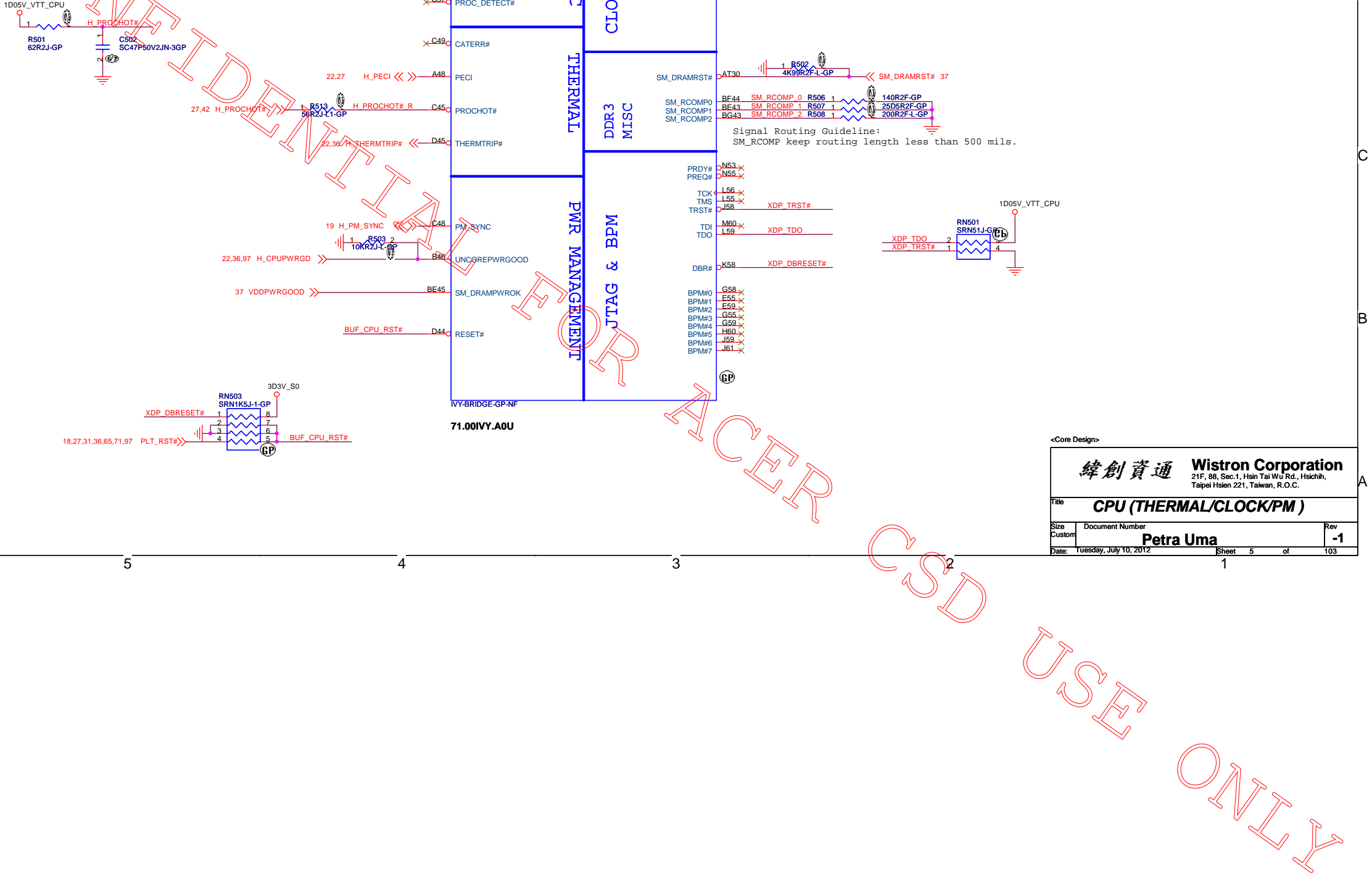
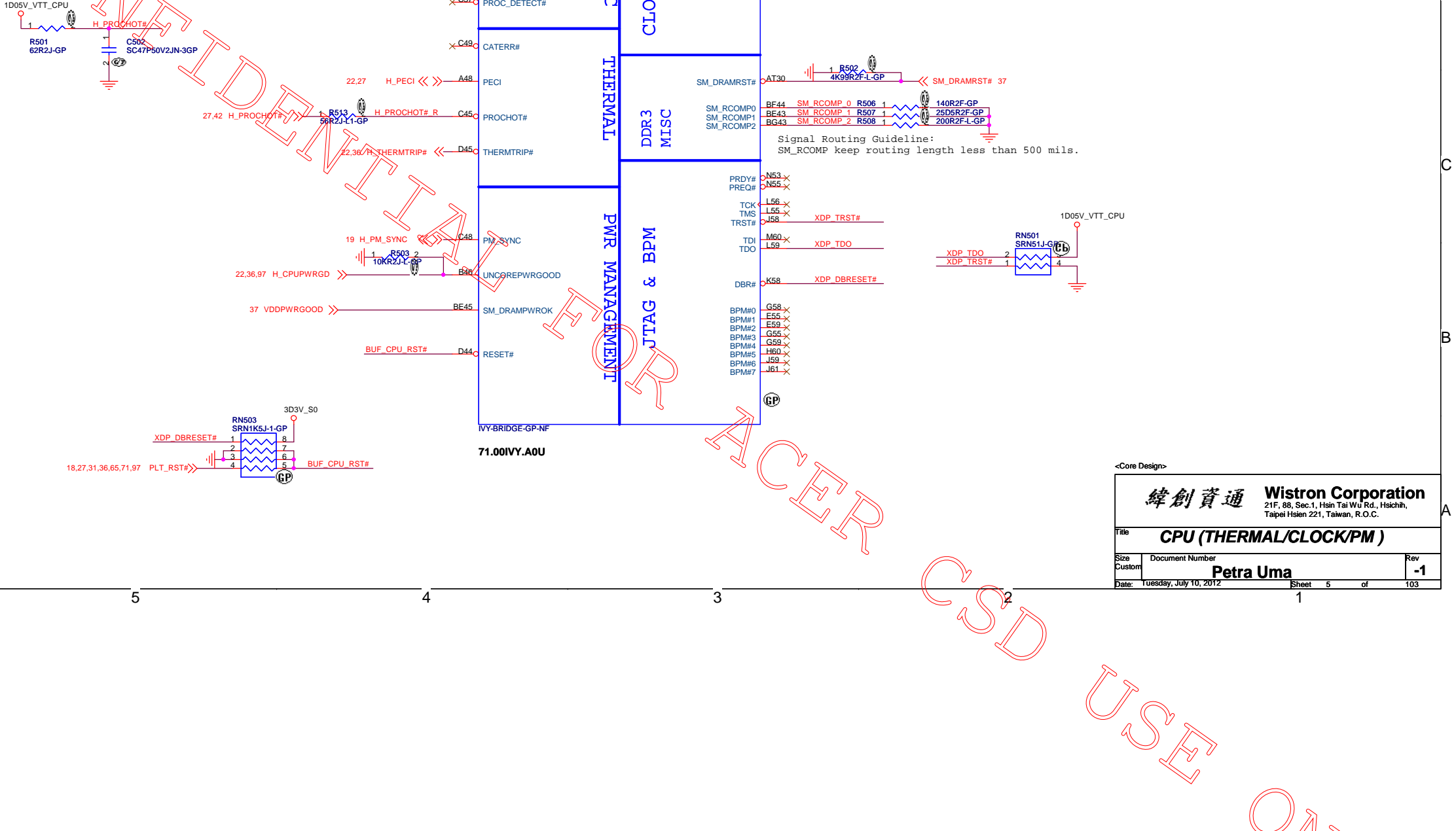
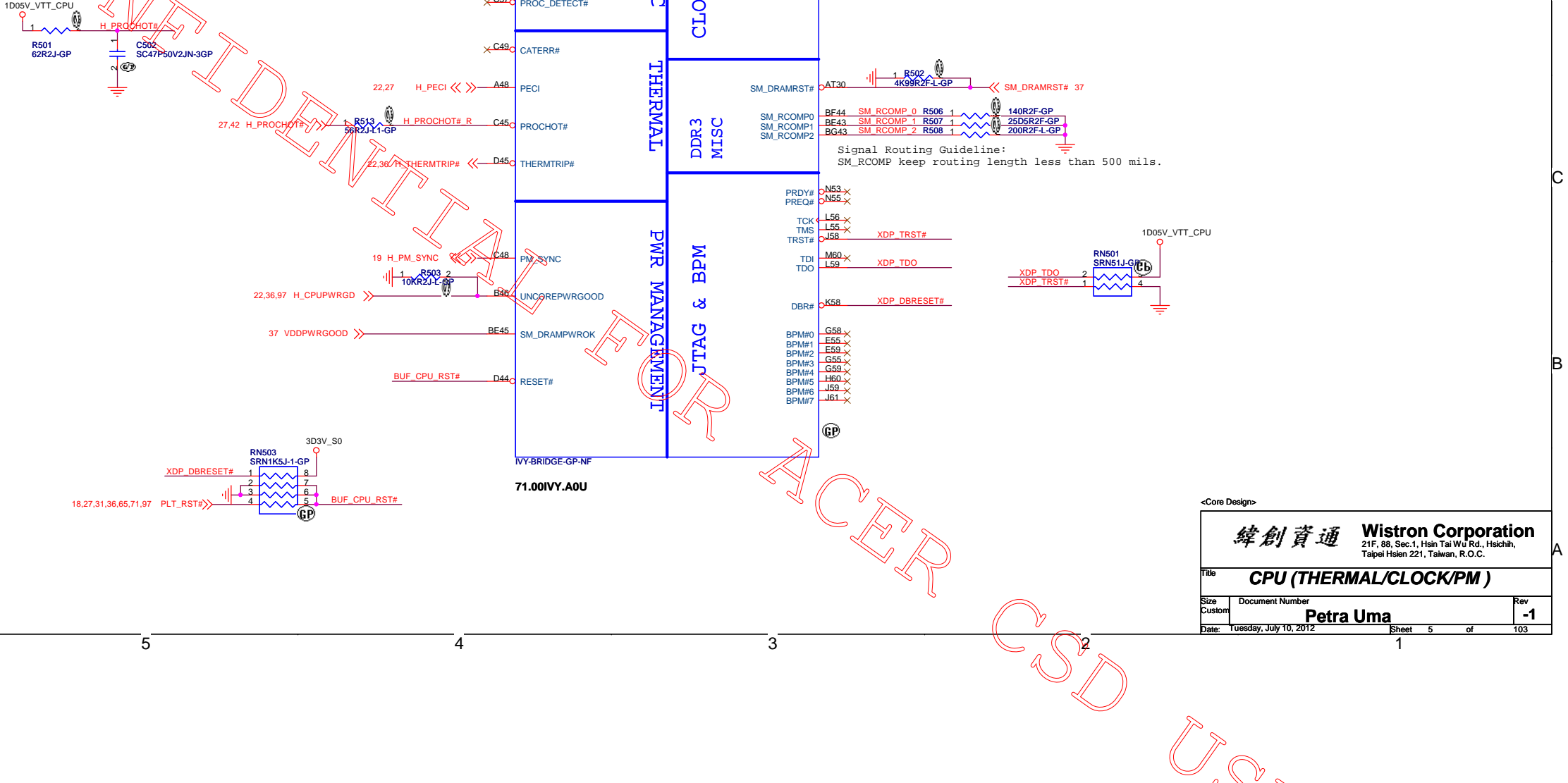
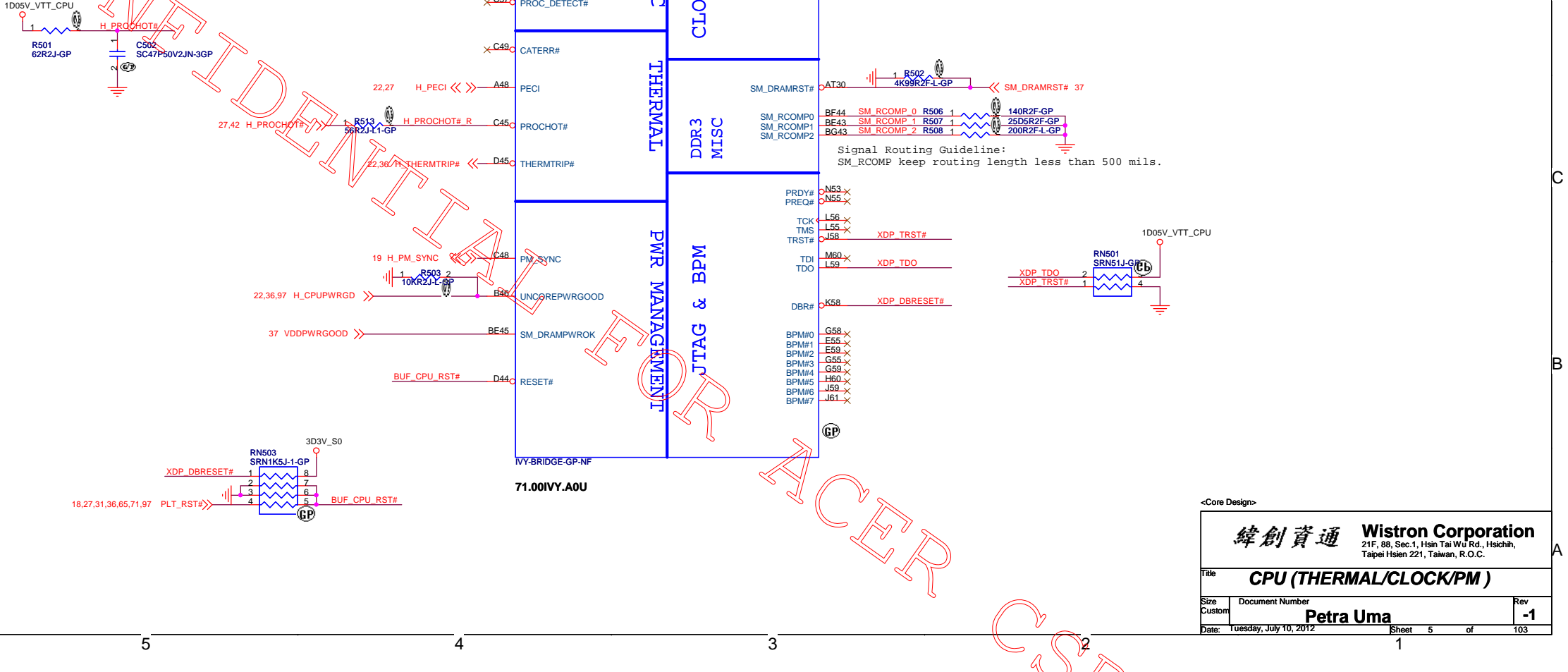
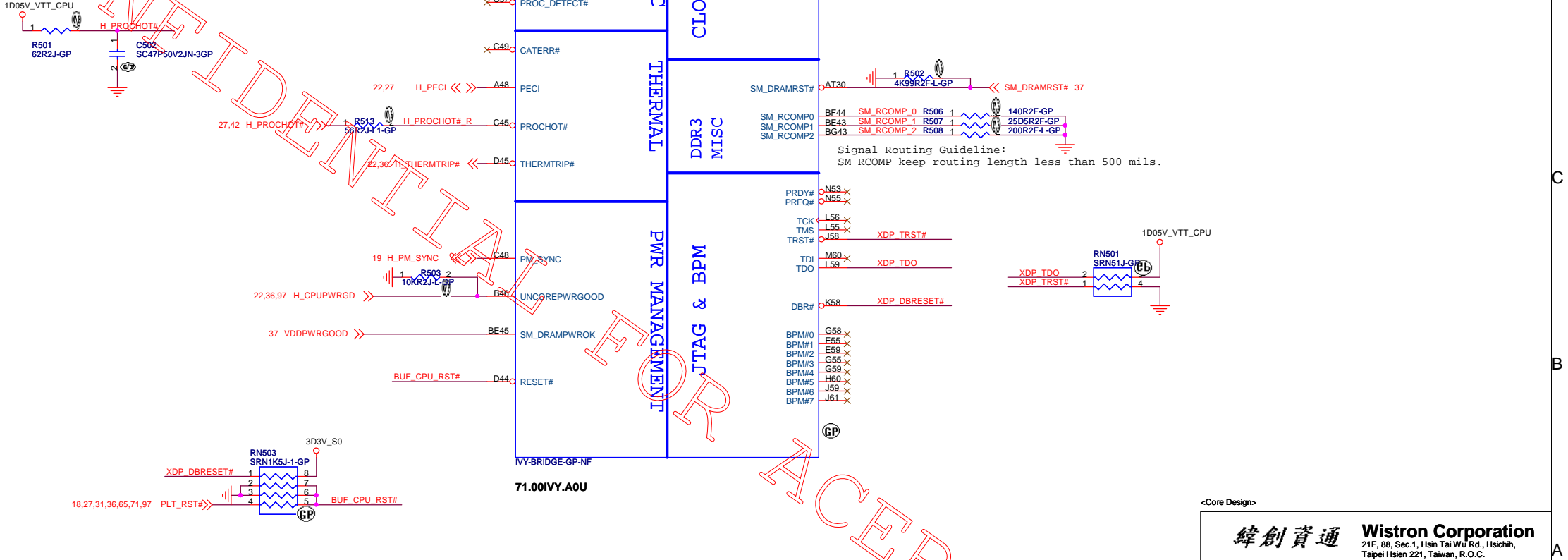
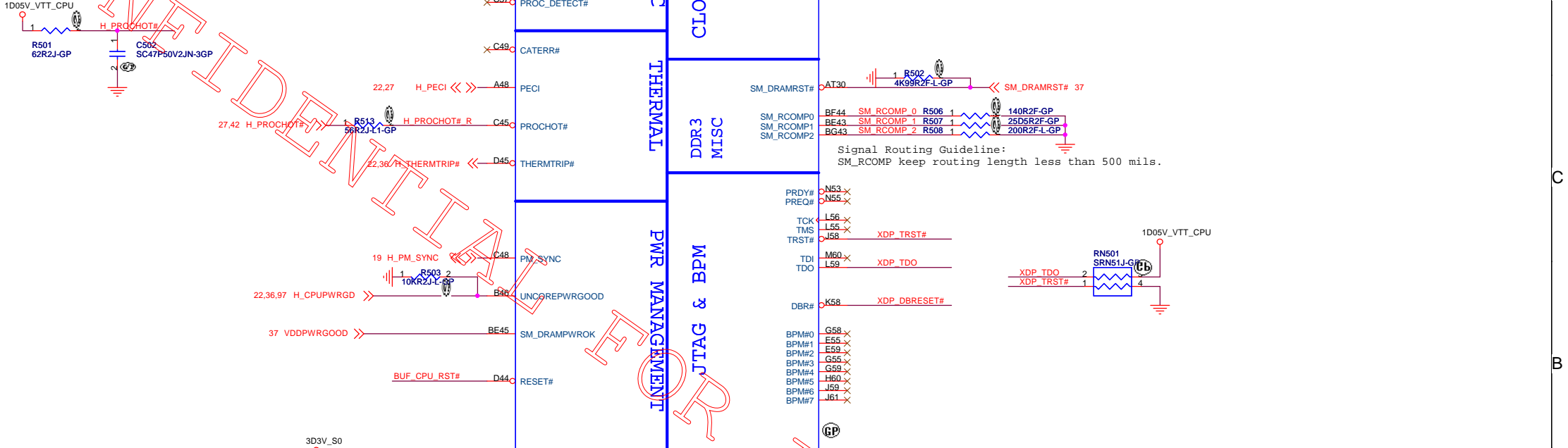
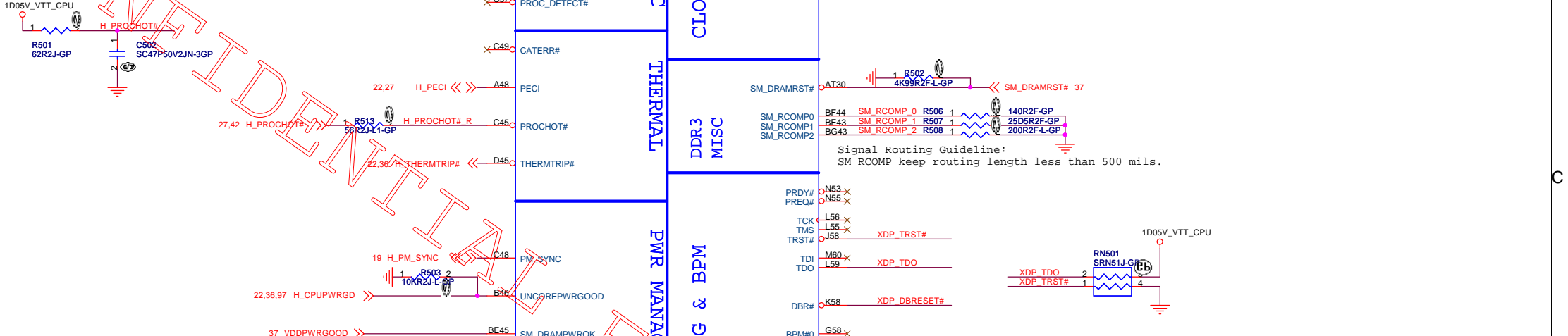
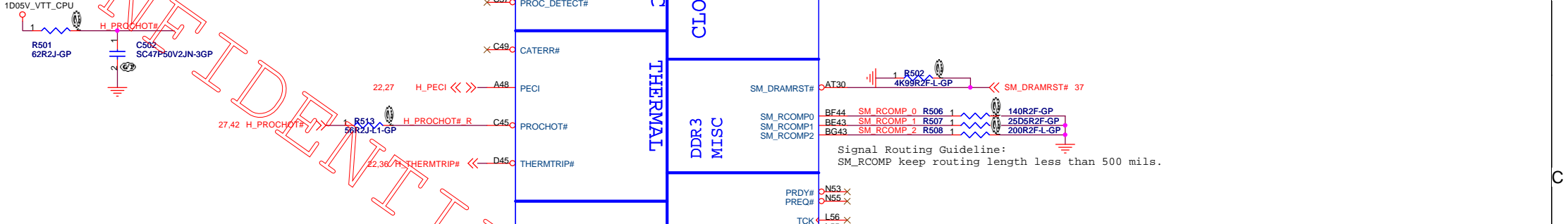
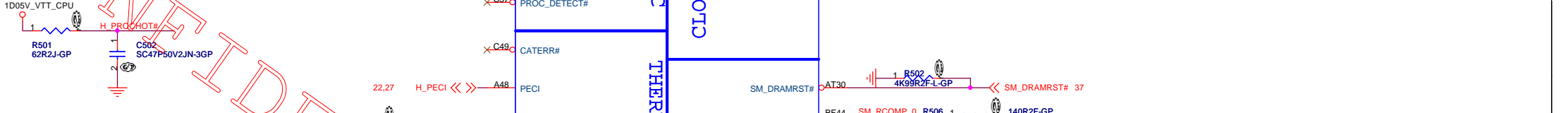
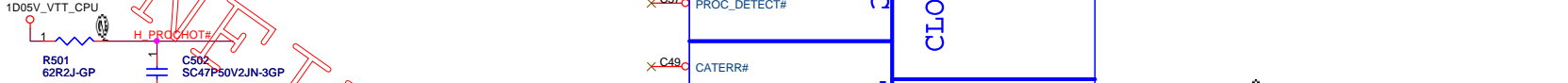
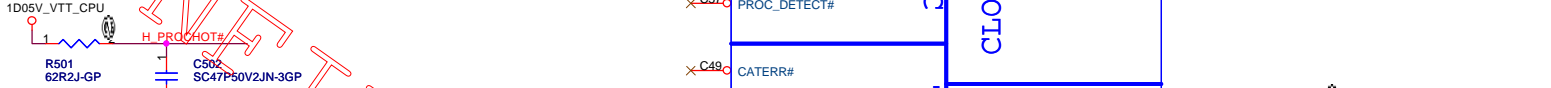
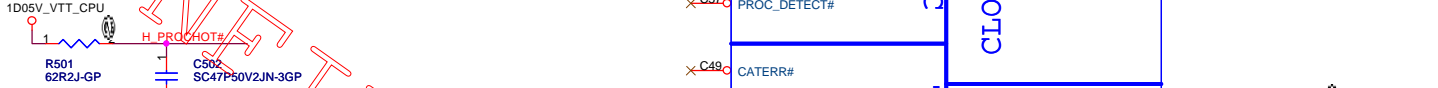
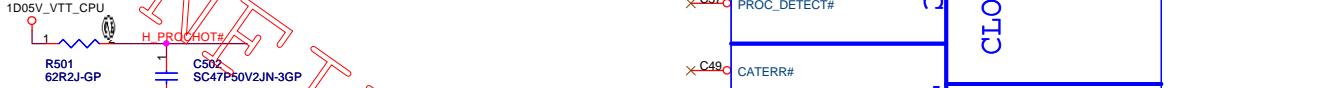
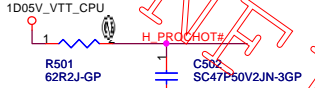
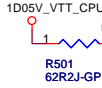
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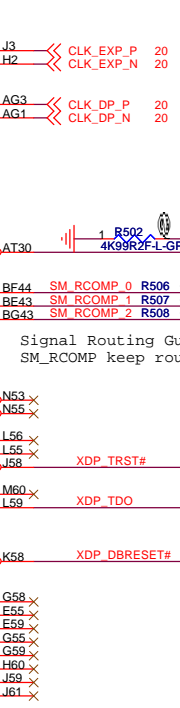
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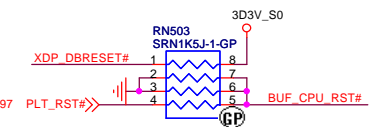
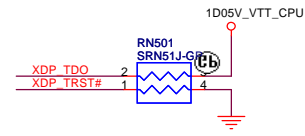
SSID = CPU



71.00IVY.A0U



Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.



<Core Design>		
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Title CPU (THERMAL/CLOCK/PM)		
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SSID = CPU

CPU1C

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M_A_DQ2 AP11 SA_DQ2
M_A_DQ3 AL10 SA_DQ3
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M_A_DQ5 AJ8 SA_DQ5
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SA_CKE0 AY26 M_A_DIM0_CKE0 14

SA_CK1 AT40 M_A_DIM0_CLK_DDR1 14
SA_CK#1 AU40 M_A_DIM0_CLK_DDR#1 14
SA_CKE1 BB26 M_A_DIM0_CKE1 14

SA_CS#0 BB40 M_A_DIM0_CS#0 14
SA_CS#1 BC41 M_A_DIM0_CS#1 14

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SA_ODT1 BA41 M_A_DIM0_ODT1 14

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SA_MA7 AT32 M_A_A7 14
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SA_BS1 BE36
SA_BS2 BA28

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14 M_A_BS1
14 M_A_BS2

14 M_A_CAS#
14 M_A_RAS#
14 M_A_WE#

IVY-BRIDGE-GP-NF

71.00IVY.A0U

CPU1D

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SB_CKE0 AR22 M_B_DIM0_CKE0 15

SB_CK1 BA36 M_B_DIM0_CLK_DDR1 15
SB_CK#1 BB36 M_B_DIM0_CLK_DDR#1 15
SB_CKE1 BE27 M_B_DIM0_CKE1 15

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15 M_B_BS2

15 M_B_CAS#
15 M_B_RAS#
15 M_B_WE#

IVY-BRIDGE-GP-NF

71.00IVY.A0U

<Core Design>

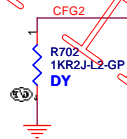
緯創資通 Wistron Corporation
21F, 28, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title CPU (DDR)
Size A3 Document Number Petra Uma
Date Tuesday, July 10, 2012 Sheet 6 of 103

SSID = CPU

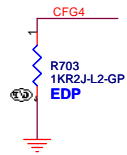
PEG Static Lane Reversal

CFG2 1: Normal Operation; Lane # definition matches socket pin map definition
0: Lane Reversed



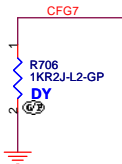
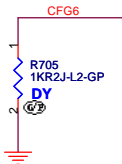
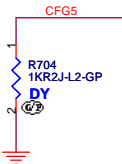
Enabl EDP function

CFG4 1: Disable
0: Enable



PCIe Port Bifurcation Straps

CFG[6:5] 11: x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

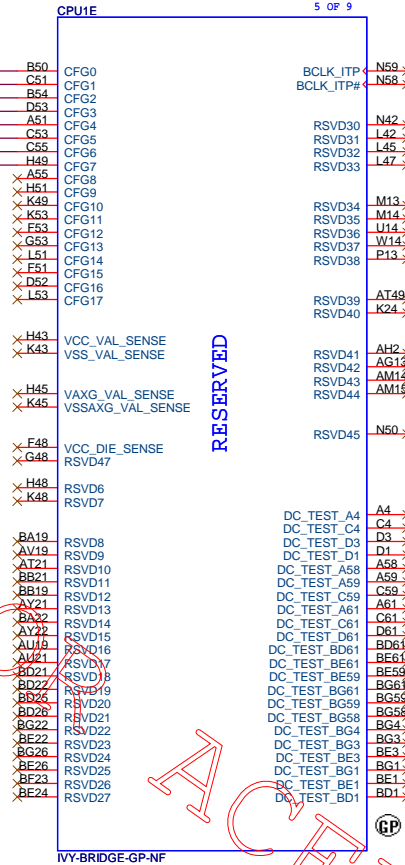


PEG DEFER TRAINING

CFG7 1: PEG Train immediately following xxRESETB de assertion
0: PEG Wait for BIOS for training

TPAD14-OP-GP TP701
TPAD14-OP-GP TP702
TPAD14-OP-GP TP703

CFG0 TP B50
CFG1 TP C51
CFG2 TP B54
CFG3 TP D53
CFG4 A51
CFG5 C53
CFG6 C55
CFG7 H49



71.00IVY.A0U

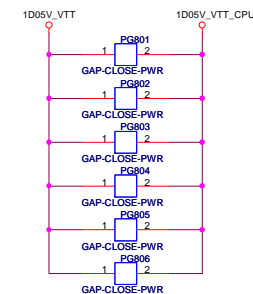
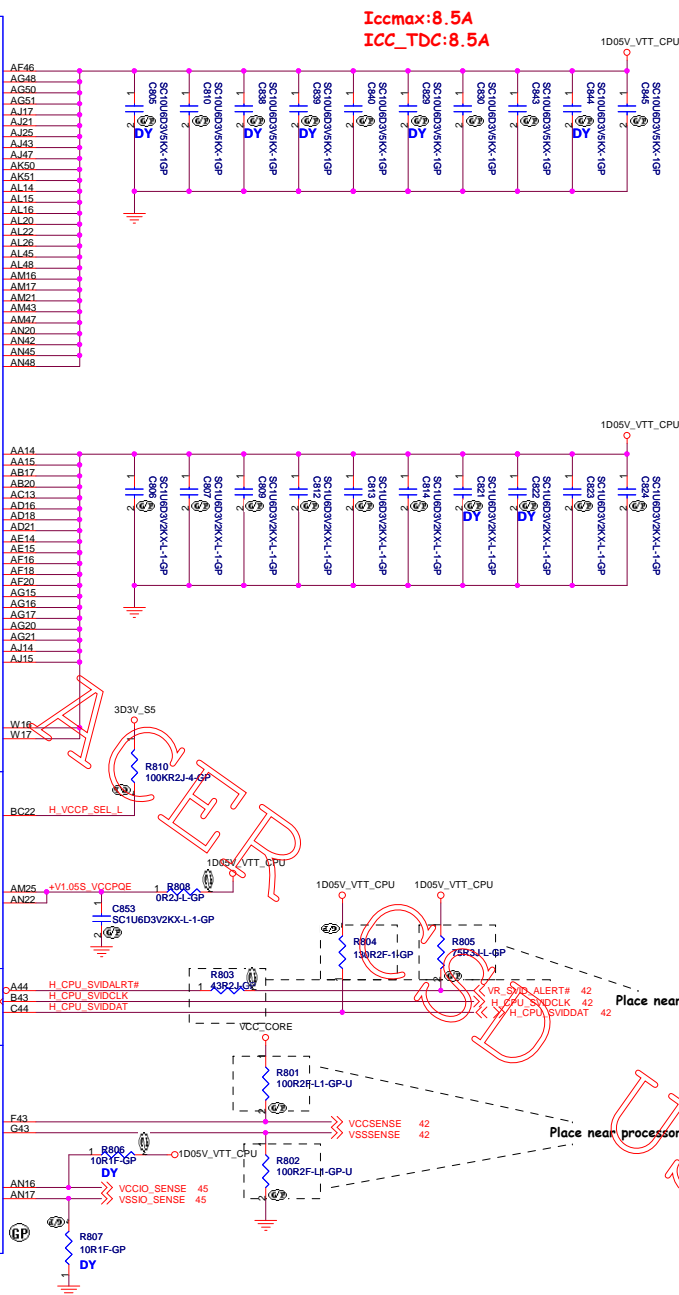
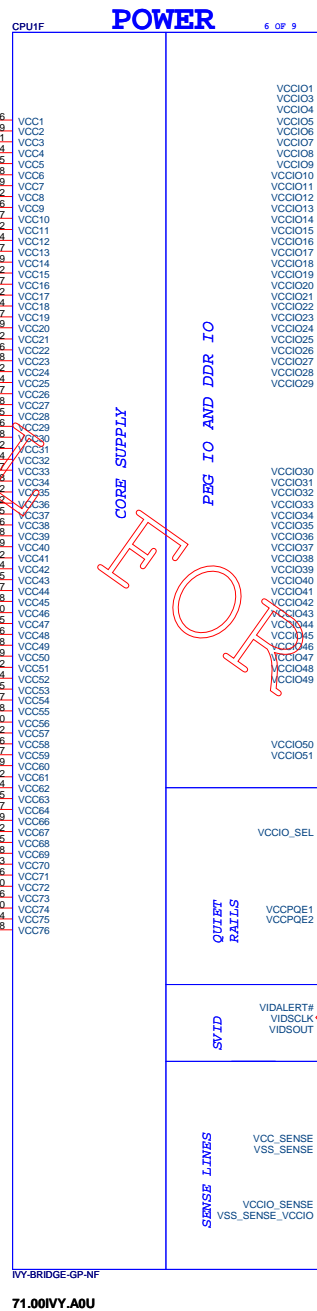
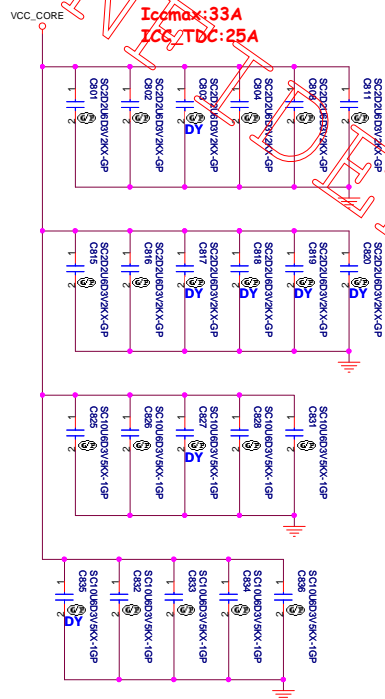
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Title CPU (RESERVED)
Size A3 Document Number Petra Uma Rev -1
Date: Wednesday, February 29, 2012 Sheet 7 of 103

SSID = CPU

ULV:17W
Iccmax:33A
ICC TDC:25A



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				CPU (VCC CORE)				Rev	
Size Custom		Document Number						Rev	
		Petra Urna						-1	
Date:		Tuesday, July 10, 2012				Sheet: 8		of 103	

SSID = CPU

Iccmax:18A(6T1)
ICC_TDC:12A(6T1)

POWER

CPU1G

7 0P 9

SM_VREF

SA_DIMM_VREFDQ

SB_DIMM_VREFDQ

AA46

AA47

AB50

AB51

AB52

AB53

AB55

AB56

AB58

AB59

AC61

AD47

AD48

AD50

AD51

AD52

AD53

AD55

AD56

AD58

AD59

AE46

AE48

AE49

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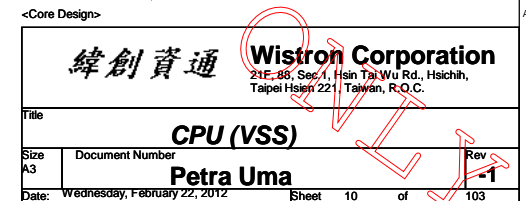
AE410

AE411

AE412

AE413

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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

XDP

Size
A4

Document Number

Petra Uma

Rev

-1

Date: Wednesday, February 22, 2012

Sheet 11 of 103

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<Core Design>

緯創資通			Wistron Corporation		
			21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Reserved					
Size	Document Number				Rev
A4	Petra Uma				-1
Date: Wednesday, February 22, 2012			Sheet	12	of 103

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<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Petra Uma

Rev
-1

Date: Wednesday, February 22, 2012

Sheet 13 of 103

SSID = MEMORY

M_A_A[15:0] 6

M_A_DQS# [7:0] 6

M_A_DQS [7:0] 6

M_A_DIM0_ODT0

M_A_DIM0_ODT1

DDR_VREF_S3

M_VREF_DQ_DIMM0

15.37 DDR3_DRAMRST#

M_A A0 98
M_A A1 97
M_A A2 96
M_A A3 95
M_A A4 94
M_A A5 93
M_A A6 92
M_A A7 91
M_A A8 90
M_A A9 89
M_A A10 88
M_A A11 87
M_A A12 86
M_A A13 85
M_A A14 84
M_A A15 83

M_A BS2

M_A BS0

M_A BS1

M_A_DQ [8:0]

M_A DQ0 5
M_A DQ1 7
M_A DQ2 15
M_A DQ3 17
M_A DQ4 4
M_A DQ5 6
M_A DQ6 16

M_A DQ7 18

M_A DQ8 21

M_A DQ9 23

M_A DQ10 35

M_A DQ11 37

M_A DQ12 39

M_A DQ13 41

M_A DQ14 51

M_A DQ15 53

M_A DQ16 55

M_A DQ17 57

M_A DQ18 59

M_A DQ19 61

M_A DQ20 63

M_A DQ21 65

M_A DQ22 67

M_A DQ23 69

M_A DQ24 71

M_A DQ25 73

M_A DQ26 75

M_A DQ27 77

M_A DQ28 79

M_A DQ29 81

M_A DQ30 83

M_A DQ31 85

M_A DQ32 87

M_A DQ33 89

M_A DQ34 91

M_A DQ35 93

M_A DQ36 95

M_A DQ37 97

M_A DQ38 99

M_A DQ39 101

M_A DQ40 103

M_A DQ41 105

M_A DQ42 107

M_A DQ43 109

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M_A DQ46 115

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M_A DQ264 551

M_A DQ265 553

M_A DQ266 555

M_A DQ267 557

M_A DQ268 559

M_A DQ269 561

SSID = MEMORY

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6 M_B_BS2 >>>
6 M_B_BS0
6 M_B_BS1

6 M_B_DQS[7:0] 6
6 M_B_DQS[7:0] 6

6 M_B_DIM0_ODT0 >>>
6 M_B_DIM0_ODT1 >>>

DDR_VREF_S3
M_VREF_DQ_DIMM1

14.37 DDR3_DRAMRST# >>>

M_B_A0 98
M_B_A1 97
M_B_A2 96
M_B_A3 95
M_B_A4 94
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M_B_A11 87
M_B_A12 86
M_B_A13 85
M_B_A14 84
M_B_A15 83
A10/AP 107
A11 106
A12 105
A13 104
A14 103
A15 102
A16/BA2 101

M_B_DQ0 5
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M_B_DQS#62 168
M_B_DQS#63 169

ODT0 116
ODT1 120

VREF_CA 126
VREF_DQ 1

RESET# 30

VTT1 203
VTT2 204

NP1
NP2
RAS# 110
WE# 113
CAS# 115
CS0# 114
CS1# 121
CKE0 73
CKE1 74
CK0 101
CK0# 103
CK1 102
CK1# 104

DM0 28
DM1 29
DM2 30
DM3 31
DM4 32
DM5 33
DM6 34
DM7 35

SDA 200
SCL 202

EVENT# 198

VDDSPD 199

SA0 197
SA1 201

NC#1 77
NC#2 122

NC#TEST 125

VDD1 75
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VDD3 77
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VDD6 80
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VDD8 82
VDD9 83
VDD10 84
VDD11 85
VDD12 86
VDD13 87
VDD14 88
VDD15 89
VDD16 90
VDD17 91
VDD18 92

VSS 2
VSS 3
VSS 4
VSS 5
VSS 6
VSS 7
VSS 8
VSS 9
VSS 10
VSS 11
VSS 12
VSS 13
VSS 14
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VSS 97
VSS 98
VSS 99
VSS 100

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

M_B_RAS# 6
M_B_WE# 6
M_B_CAS# 6
M_B_DIM0_CS#0 6
M_B_DIM0_CS#1 6
M_B_DIM0_CKE0 6
M_B_DIM0_CKE1 6
M_B_DIM0_CLK_DDR0 6
M_B_DIM0_CLK_DDR#0 6
M_B_DIM0_CLK_DDR1 6
M_B_DIM0_CLK_DDR#1 6

PCH_SMBDATA 14.20.69
PCH_SMBCLK 14.20.69

TS#_DIMM0_1 14

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
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15V_S3

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15V_S3

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YOKR2JL-GP

15V_S3

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YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

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15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

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YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

15V_S3

SA1_DIM1 2
YOKR2JL-GP

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C1501
SCD1U10V2KX-L1-GP

SCD1U10V2KX-L1-GP
C1513
SCD1U10V2KX-L1-GP

SCD1U10V2KX-L1-GP
C1513
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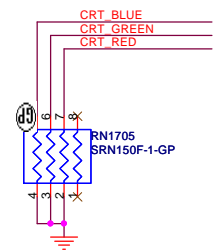
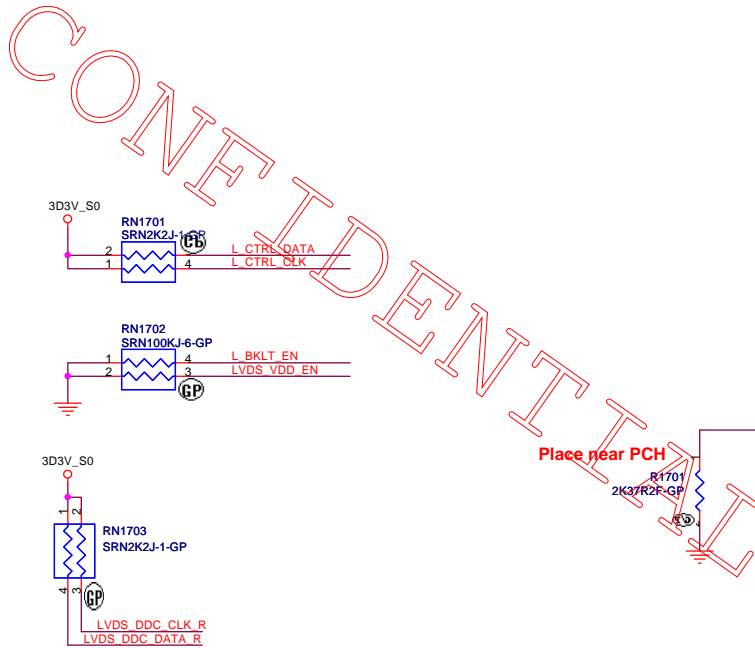
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CONFIDENTIAL FOR ACER CSD USE ONLY

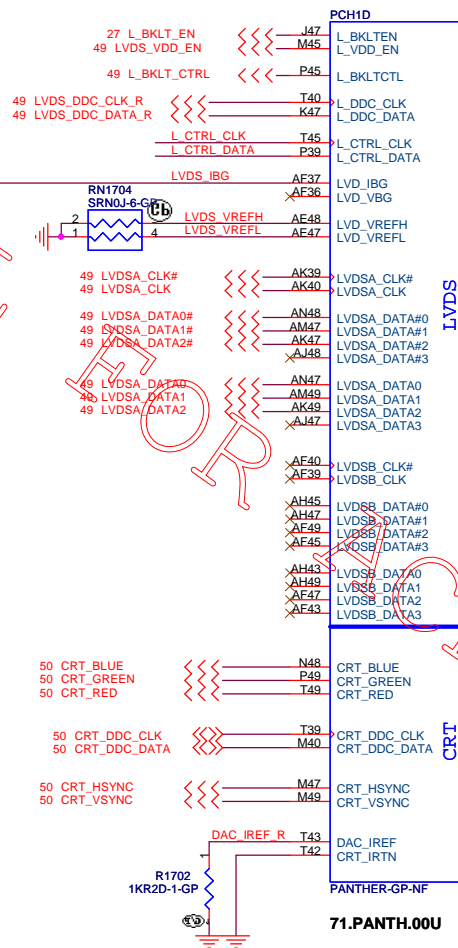
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<Core Design>

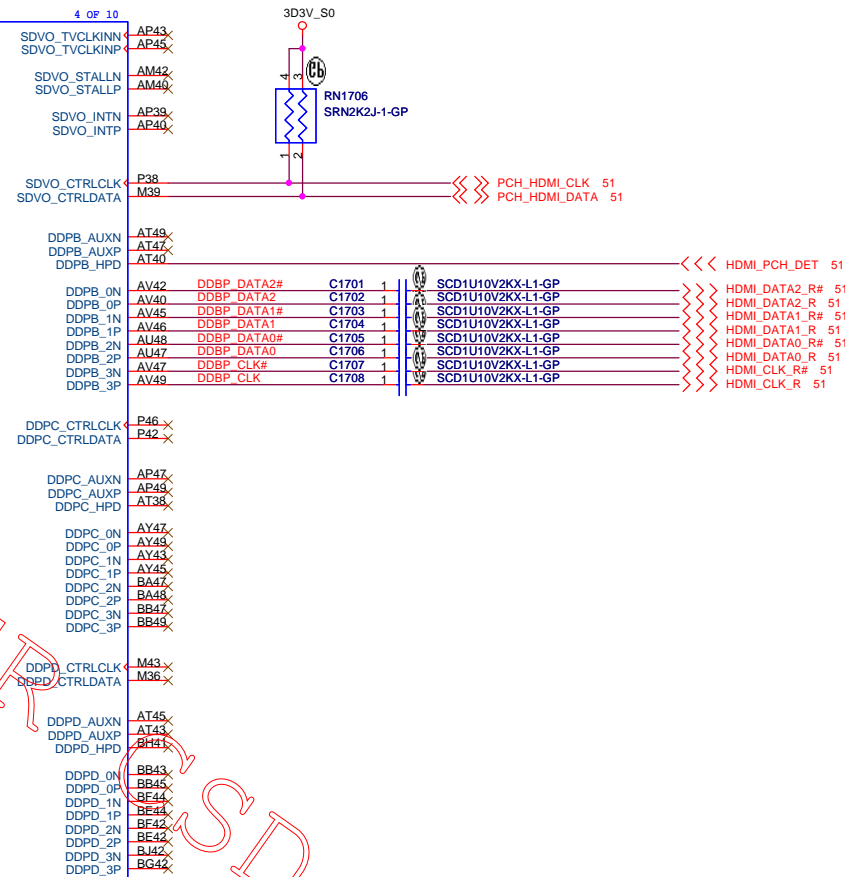
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DDR3-SODIMM2			
Size A4	Document Number Petra Uma		Rev -1
Date: Wednesday, February 22, 2012	Sheet	16 of	103



Place near PCH

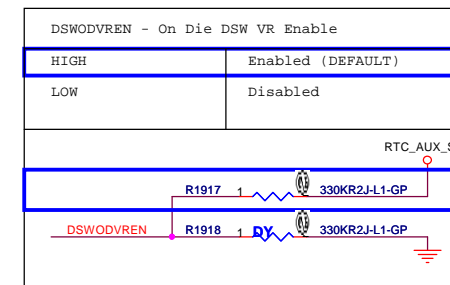


Digital Display Interface



USE

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



3D3V_S5

RN1901
SRN10KJ-6-CP

8 1
7 2
6 3
5 4

BATLOW#
PM R1#
AC PRESENT
SUS_PWR_ACK R

R1921_1
10KR2J-L-GP

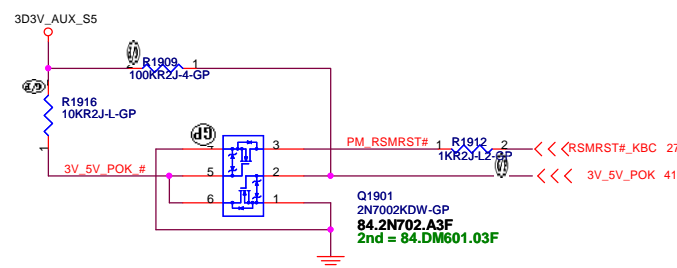
PCIE_WAKE#

R1922_1
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SUS_PWR_ACK#

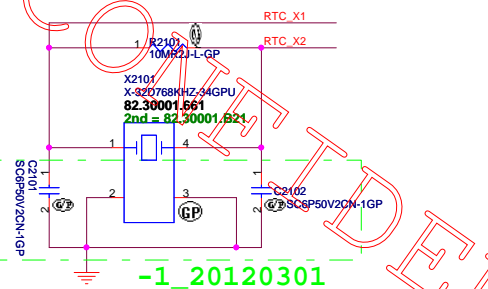
R1908_1
100KR2J-4-GP

PM RSMRST#



USE

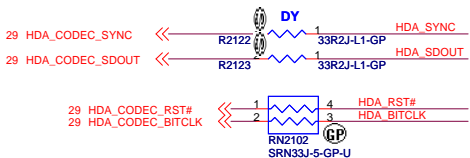
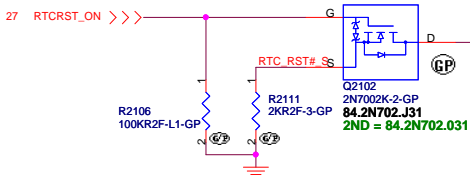
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-1_20120223

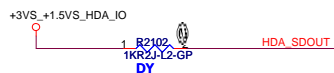
RTC Reset

INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

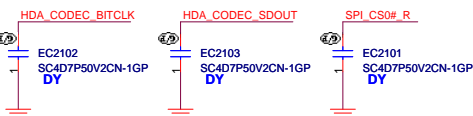
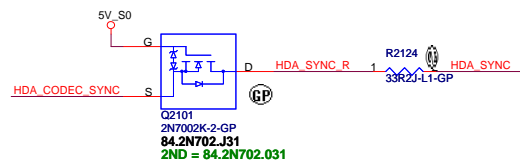
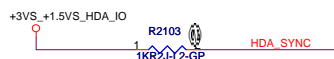


Flash Descriptor Security Override

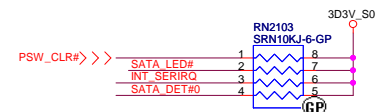
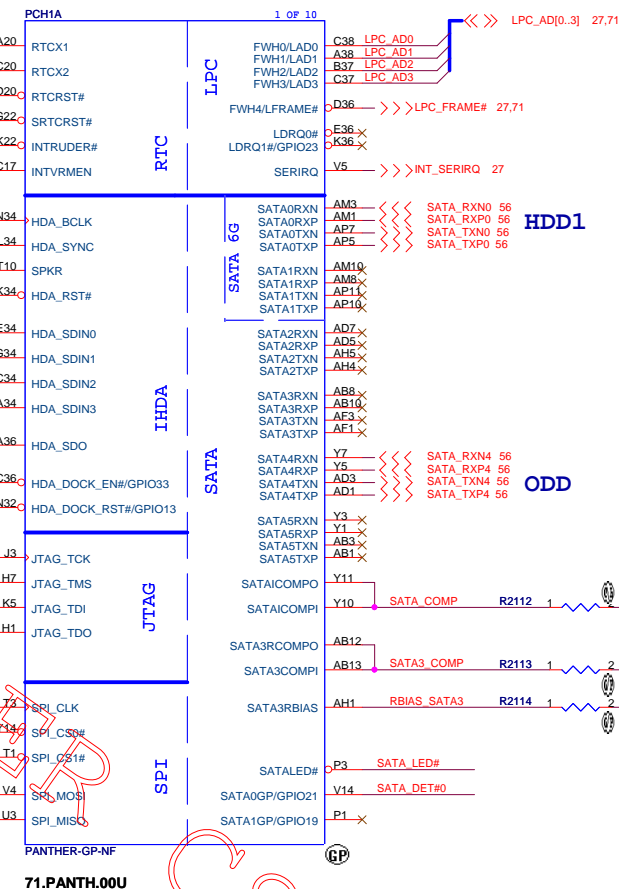
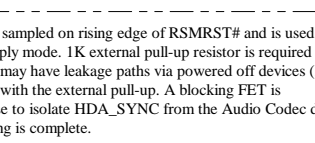
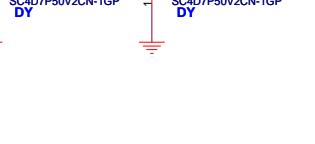
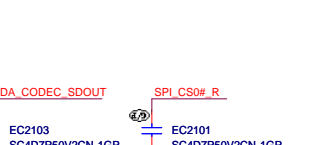
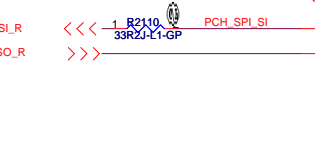
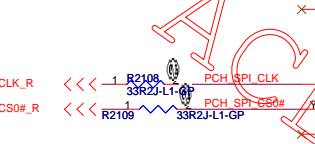
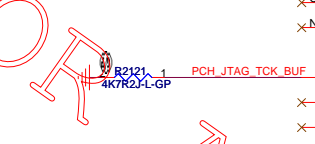
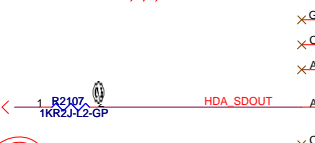
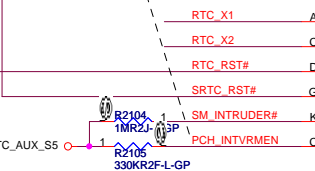
HDA_SDOUT	Low = Default High = Enable
-----------	--------------------------------



PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



USE

<Core Design>

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin-Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PCH (SPI/RTC/LPC/SATA/IHDA)	
Size Custom	Document Number
Date: Tuesday, July 10, 2012	Sheet 21 of 103

SSID = PCH

CONFIDENTIAL

Pass Word Clear

71.PANTH.00U

USE ONLY

Wistron Corporation

PCH (GPIO/CPU)

Document Number

Rev -1

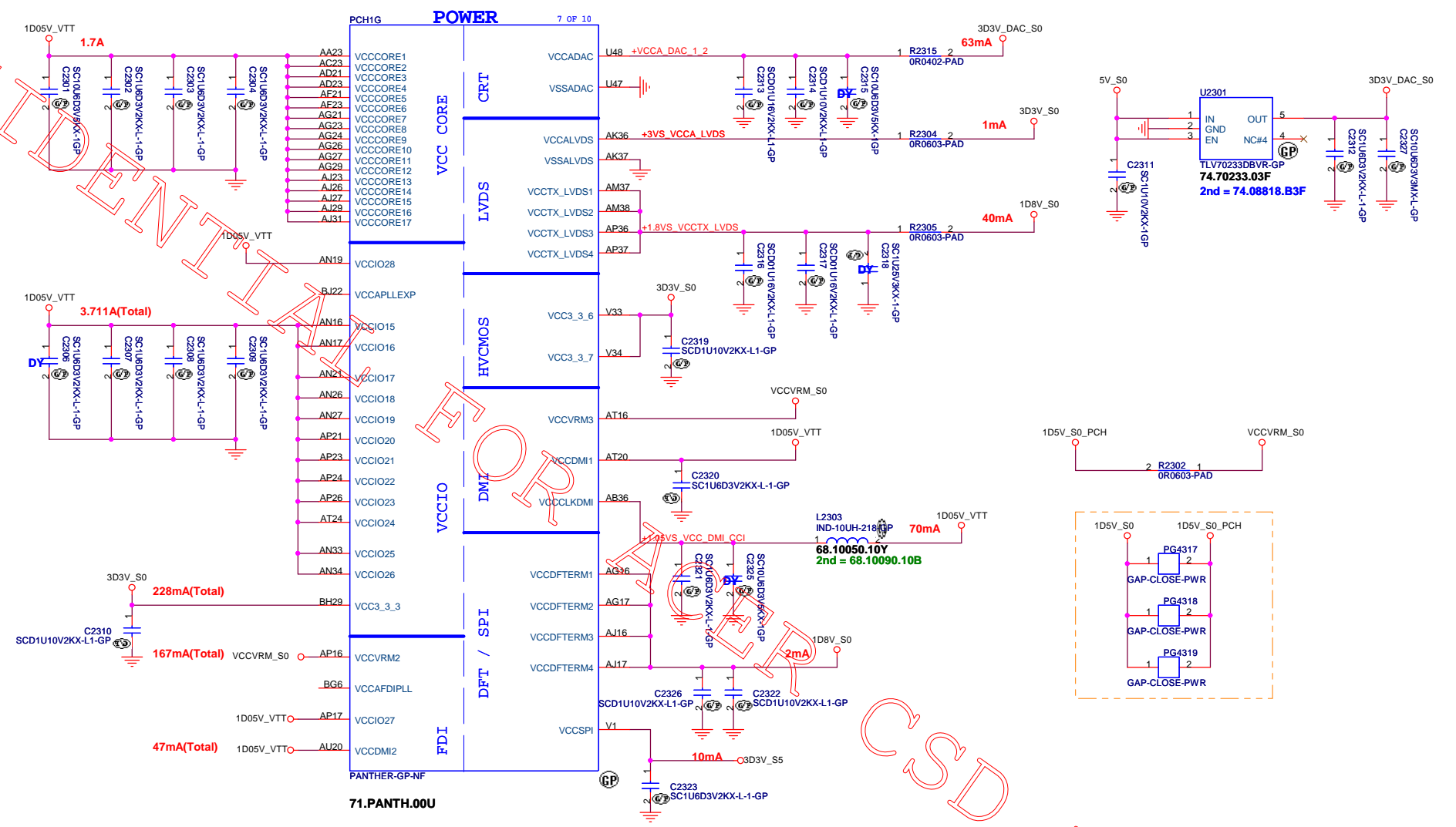
Date: Tuesday, July 10, 2012

Sheet 22 of 103

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[illegible]

SSID = PCH



USE

SSID = PCH

PCH1H

8 OF 10

H5	VSS0		
AA17	VSS1	VSS80	AK38
AA2	VSS2	VSS81	AK4
AA3	VSS3	VSS82	AK42
AA33	VSS4	VSS83	AK46
AA34	VSS5	VSS84	AK8
AB11	VSS6	AL16	
AB14	VSS7	VSS85	AL17
AB39	VSS8	VSS86	AL19
AB4	VSS9	VSS87	AL2
AB43	VSS10	VSS88	AL21
AB5	VSS11	VSS89	AL23
AB7	VSS12	VSS90	AL26
AC19	VSS13	VSS91	AL27
AC2	VSS14	VSS92	AL31
AC21	VSS15	VSS93	AL33
AC24	VSS16	VSS94	AL34
AC33	VSS17	VSS95	AL48
AC34	VSS18	VSS96	AM11
AC48	VSS19	VSS97	AM14
AD10	VSS20	VSS98	AM36
AD11	VSS21	VSS99	AM39
AD12	VSS22	VSS100	AM43
AD13	VSS23	VSS101	AM45
AD19	VSS24	VSS102	AM46
AD24	VSS25	VSS103	AM7
AD26	VSS26	VSS104	AN2
AD27	VSS27	VSS105	AN29
AD33	VSS28	VSS106	AN3
AD34	VSS29	VSS107	AN31
AD36	VSS30	VSS108	AP12
AD37	VSS31	VSS109	AP19
AD38	VSS32	VSS110	AP28
AD39	VSS33	VSS111	AP30
AD4	VSS34	VSS112	AP32
AD40	VSS35	VSS113	AP38
AD42	VSS36	VSS114	AP4
AD43	VSS37	VSS115	AP42
AD45	VSS38	VSS116	AP46
AD46	VSS39	VSS117	AP8
AD8	VSS40	VSS118	AR2
AE2	VSS41	VSS119	AR48
AE3	VSS42	VSS120	AT11
AF10	VSS43	VSS121	AT13
AF12	VSS44	VSS122	AT18
AD14	VSS45	VSS123	AT22
AD16	VSS46	VSS124	AT26
AF16	VSS47	VSS125	AT28
AF19	VSS48	VSS126	AT30
AF24	VSS49	VSS127	AT32
AF26	VSS50	VSS128	AT34
AF27	VSS51	VSS129	AT39
AF29	VSS52	VSS130	AT42
AF31	VSS53	VSS131	AT46
AF38	VSS54	VSS132	AT7
AF4	VSS55	VSS133	AT7
AF42	VSS56	VSS134	AU24
AF46	VSS57	VSS135	AU30
AF5	VSS58	VSS136	AV16
AF7	VSS59	VSS137	AV20
AF8	VSS60	VSS138	AV24
AG19	VSS61	VSS139	AV30
AG2	VSS62	VSS140	AV38
AG31	VSS63	VSS141	AV4
AG48	VSS64	VSS142	AV43
AH11	VSS65	VSS143	AV8
AH3	VSS66	VSS144	AW14
AH36	VSS67	VSS145	AW18
AH39	VSS68	VSS146	AW2
AH40	VSS69	VSS147	AW22
AH42	VSS70	VSS148	AW26
AH46	VSS71	VSS149	AW28
AH7	VSS72	VSS150	AW34
AJ19	VSS73	VSS151	AW36
AJ21	VSS74	VSS152	AW40
AJ24	VSS75	VSS153	AW48
AJ33	VSS76	VSS154	AW48
AJ34	VSS77	VSS155	AV11
AK12	VSS78	VSS156	AY12
AK3	VSS79	VSS157	AY28
		VSS158	AY28

PANTHER-GP-NF

71.PANTH.00U

PCH1I

9 OF 10

AY4	VSS159	VSS259	H46
AY42	VSS160	VSS260	K18
AY46	VSS161	VSS261	K26
AY4	VSS162	VSS262	K38
B11	VSS163	VSS263	K46
B15	VSS164	VSS264	K7
B19	VSS165	VSS265	L18
B23	VSS166	VSS266	L2
B27	VSS167	VSS267	L20
B31	VSS168	VSS268	L26
B35	VSS169	VSS269	L28
B39	VSS170	VSS270	L36
B7	VSS171	VSS271	L48
F45	VSS172	VSS272	M12
BB12	VSS173	VSS273	P16
BB16	VSS174	VSS274	M18
BB20	VSS175	VSS275	M22
BB22	VSS176	VSS276	M24
BB24	VSS177	VSS277	M30
BB28	VSS178	VSS278	M32
BB30	VSS179	VSS279	M34
BB38	VSS180	VSS280	M38
BB4	VSS181	VSS281	M4
BB46	VSS182	VSS282	M42
BC14	VSS183	VSS283	M46
BC18	VSS184	VSS284	M8
BC2	VSS185	VSS285	N18
BC22	VSS186	VSS286	P30
BC26	VSS187	VSS287	N47
BC32	VSS188	VSS288	P11
BC34	VSS189	VSS289	P18
BC36	VSS190	VSS290	T33
BC40	VSS191	VSS291	P40
BC42	VSS192	VSS292	P43
BC48	VSS193	VSS293	P47
BD46	VSS194	VSS294	P7
BD5	VSS195	VSS295	R2
BE22	VSS196	VSS296	R48
BE26	VSS197	VSS297	T12
BE40	VSS198	VSS298	T31
BE10	VSS199	VSS299	T37
BE12	VSS200	VSS300	T4
BE16	VSS201	VSS301	W34
BE20	VSS202	VSS302	T46
BE22	VSS203	VSS303	T47
BE24	VSS204	VSS304	T8
BE26	VSS205	VSS305	V11
BE28	VSS206	VSS306	V17
BD3	VSS207	VSS307	V26
BE30	VSS208	VSS308	V27
BE38	VSS209	VSS309	V29
BF40	VSS210	VSS310	V31
BFR	VSS211	VSS311	V36
BG17	VSS212	VSS312	V39
BG21	VSS213	VSS313	V43
BG33	VSS214	VSS314	V7
BG44	VSS215	VSS315	W17
BG8	VSS216	VSS316	W19
BH11	VSS217	VSS317	W2
BH15	VSS218	VSS318	W27
BH17	VSS219	VSS319	W48
BH19	VSS220	VSS320	Y12
H10	VSS221	VSS321	Y38
BH27	VSS222	VSS322	Y4
BH31	VSS223	VSS323	Y42
BH33	VSS224	VSS324	Y46
BH35	VSS225	VSS325	Y8
BH39	VSS226	VSS326	BG29
BH43	VSS227	VSS327	N24
BH7	VSS228	VSS328	AJ3
D3	VSS229	VSS329	AD47
D12	VSS230	VSS330	B43
D16	VSS231	VSS331	BE10
D18	VSS232	VSS332	BE10
D22	VSS233	VSS333	BG41
D24	VSS234	VSS334	G14
D26	VSS235	VSS335	H16
D30	VSS236	VSS336	T36
D32	VSS237	VSS337	BG22
D34	VSS238	VSS338	BG24
D38	VSS239	VSS339	C22
D42	VSS240	VSS340	AP13
D8	VSS241	VSS341	M14
E18	VSS242	VSS342	AP3
E26	VSS243	VSS343	AP1
G18	VSS244	VSS344	BE16
G20	VSS245	VSS345	BC16
G26	VSS246	VSS346	BG28
G28	VSS247	VSS347	BJ28
G36	VSS248	VSS348	
G48	VSS249	VSS349	
H12	VSS250	VSS350	
H18	VSS251	VSS351	
H22	VSS252	VSS352	
H24	VSS253		
H26	VSS254		
H30	VSS255		
H32	VSS256		
H34	VSS257		
F3	VSS258		

PANTHER-GP-NF

71.PANTH.00U

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
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Title			PCH (VSS)
Size	Document Number	Rev	-1
A3	Petra Uma		
Date:	Wednesday, February 22, 2012	Sheet	25 of 103

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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Clock(colay)			
Size	Document Number		Rev
A4	Petra Uma		-1
Date: Wednesday, February 22, 2012		Sheet	26 of 103

A

Low R

4

82709
 100K244-GP
 DY
 ②

82710
 100K244-GP
 DY
 ②

DISCRETE# will change to internal pull up

US

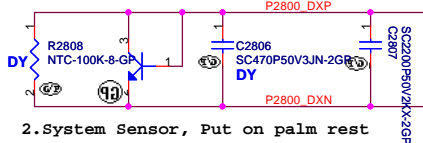


SSID = Thermal

Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

Q2801
PMBS3904-1-GP
84.03904.L06
2nd = 84.03904.T11



2.System Sensor, Put on palm rest

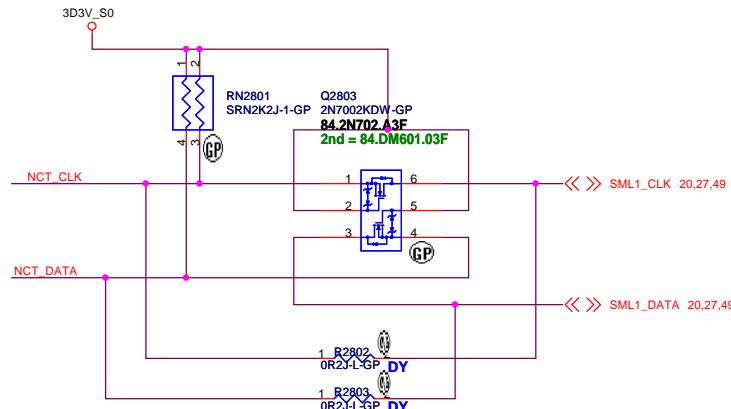
1.H/W T8 Shutdown

ALERT# /T CRIT#
Pull-up Resistor

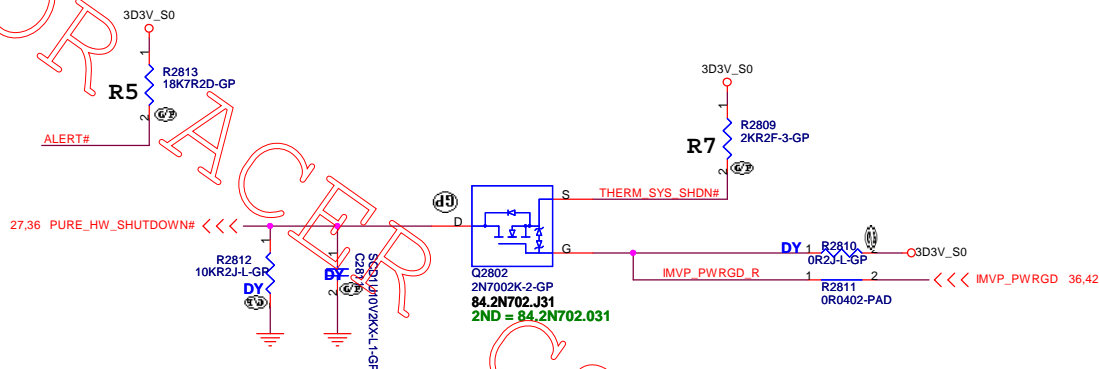
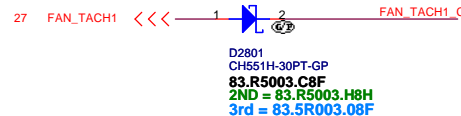
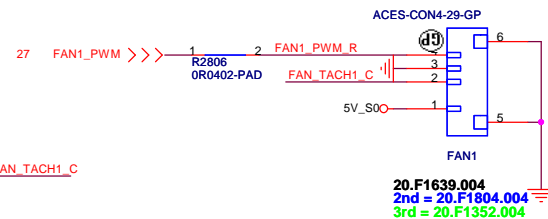
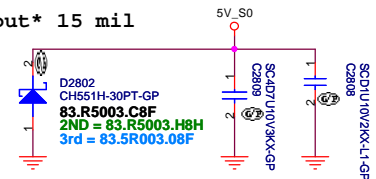
	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5	2Kohm	77°C	87°C	97°C	107°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

SB T8=85 degree



Layout 15 mil



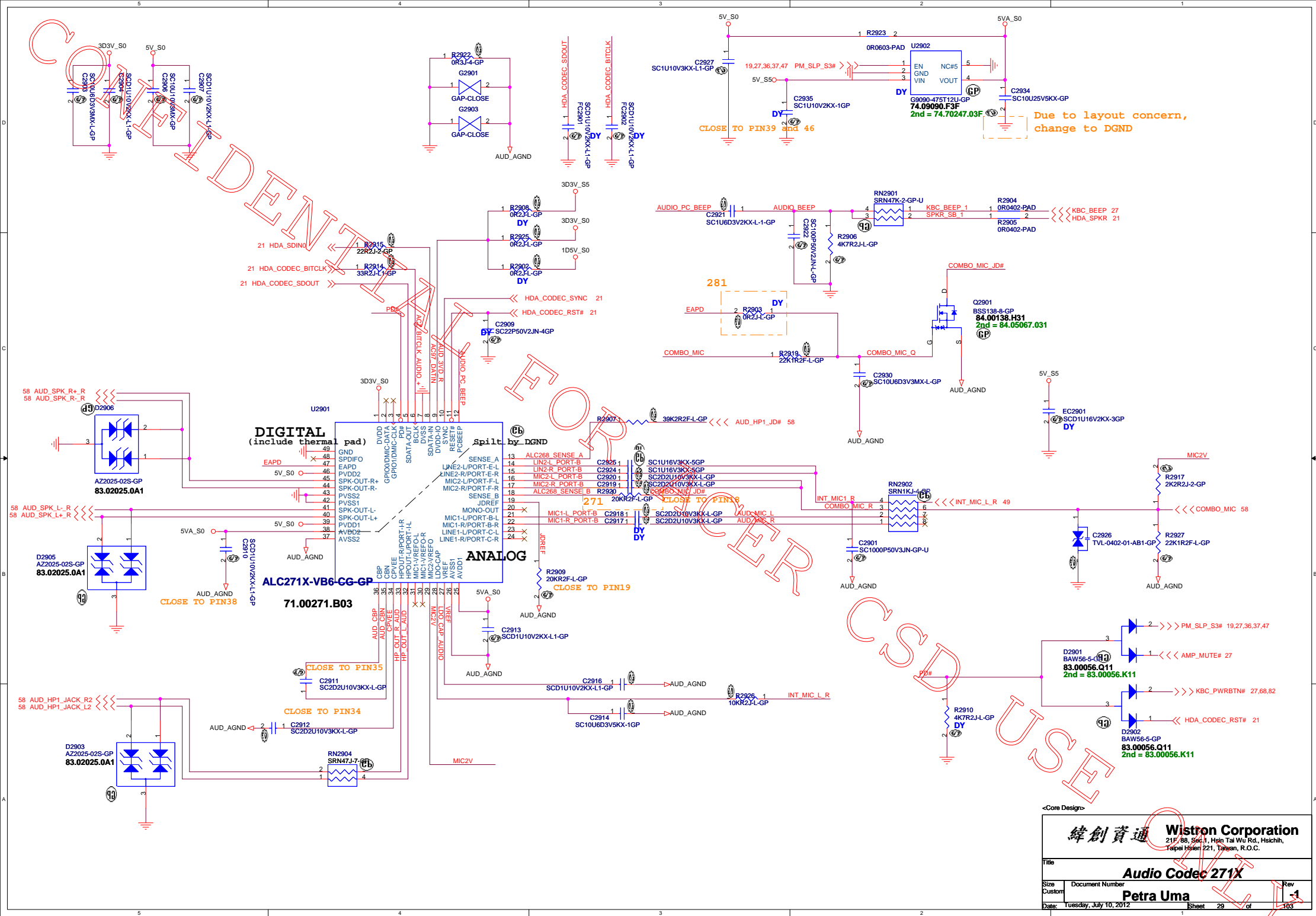
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緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
Thermal 7718/Fan Controllor P2793			
Size	Document Number		Rev
Custom	Petra Uma		-1
Date:	Tuesday, July 10, 2012		
	Sheet 28	of	103

ONLY



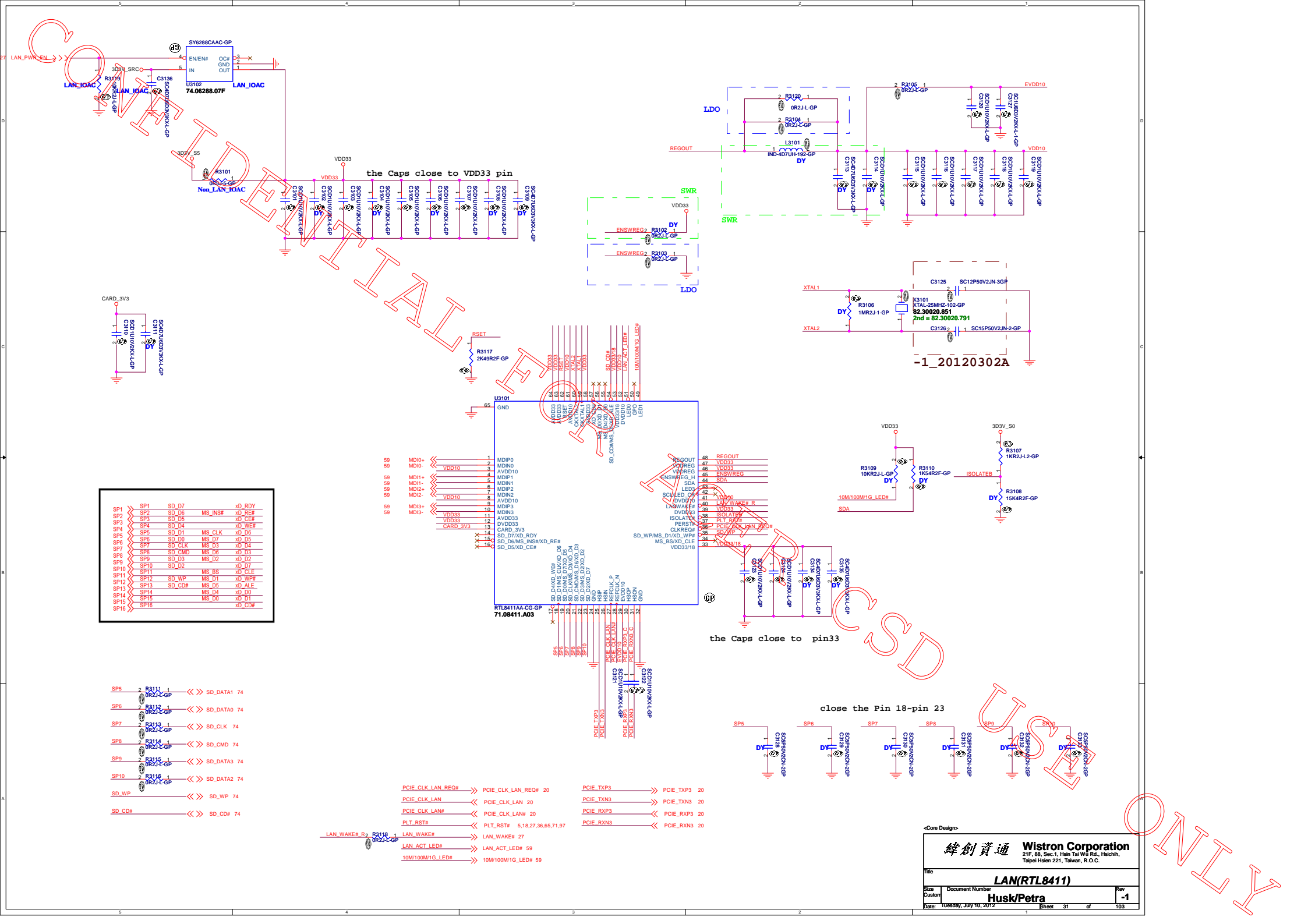
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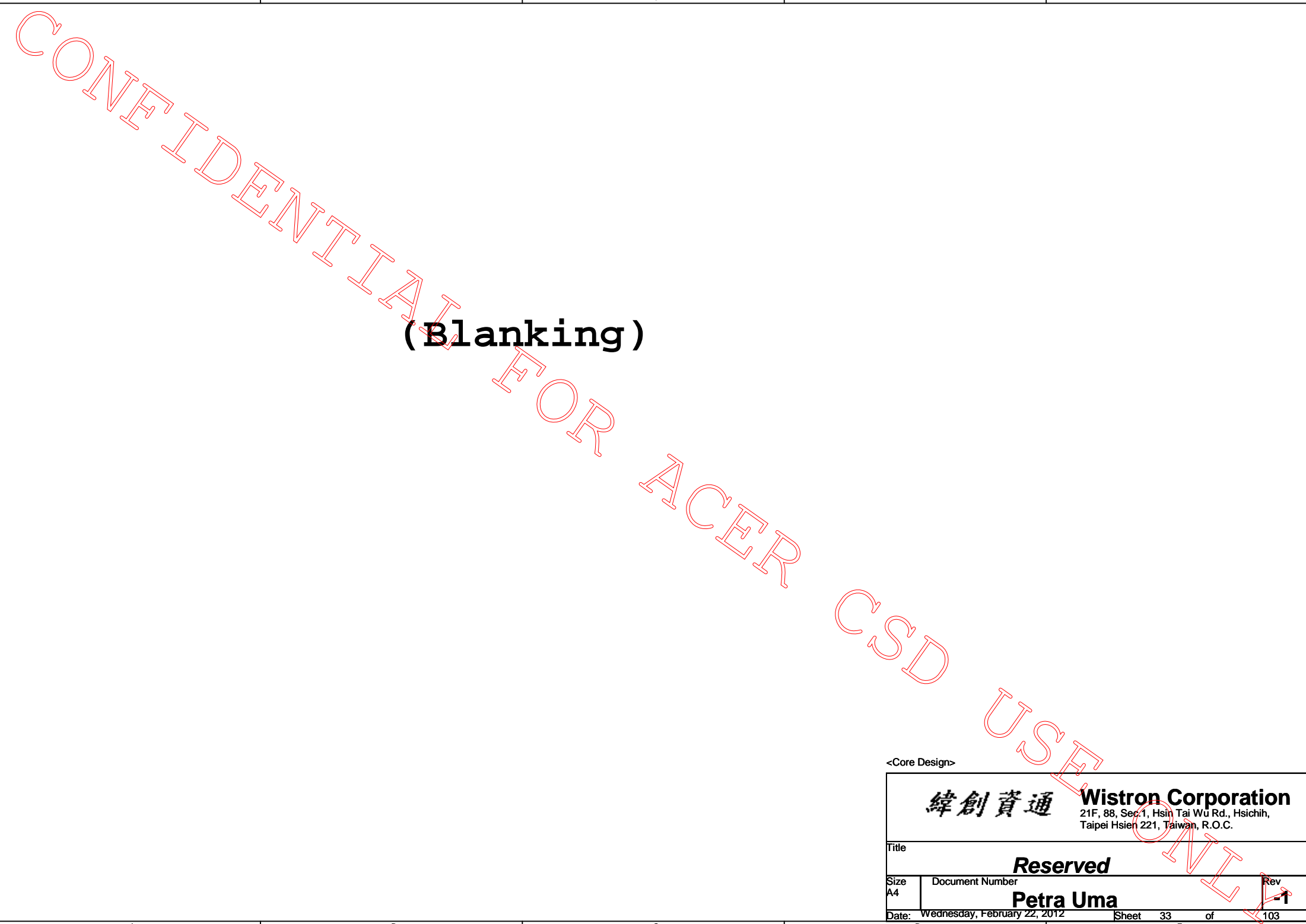
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Audio AMP			
Size	Document Number		Rev
A4	Petra Uma		-1
Date: Wednesday, February 22, 2012		Sheet	30 of 103



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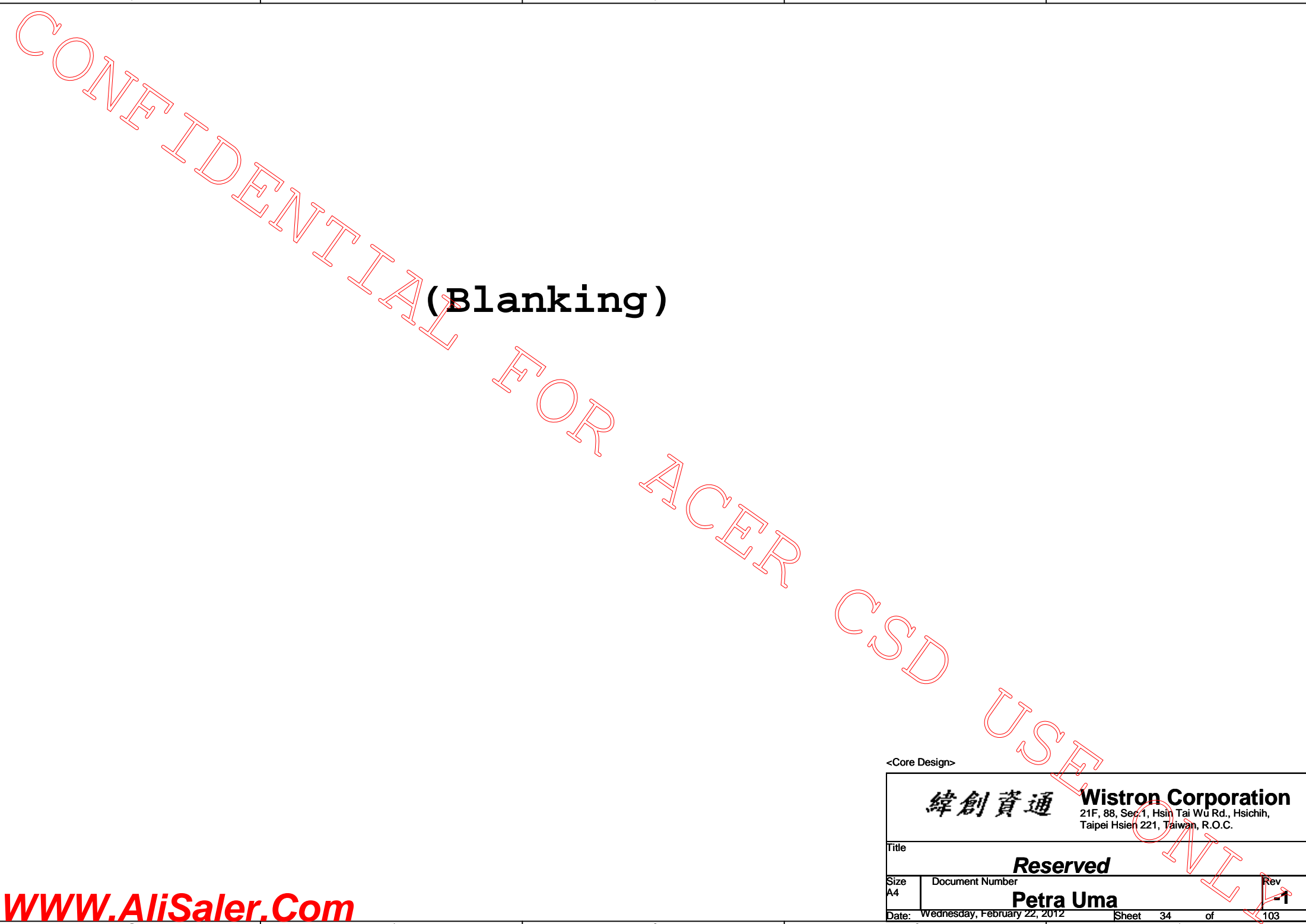
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RTS5159 (CARD READER)			
Size A4	Document Number Petra Uma		Rev -1
Date: Wednesday, February 22, 2012		Sheet 32 of	103



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<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Petra Uma</div>	Rev <div>-1</div>
Date: Wednesday, February 22, 2012		Sheet 33 of 103



<Core Design>

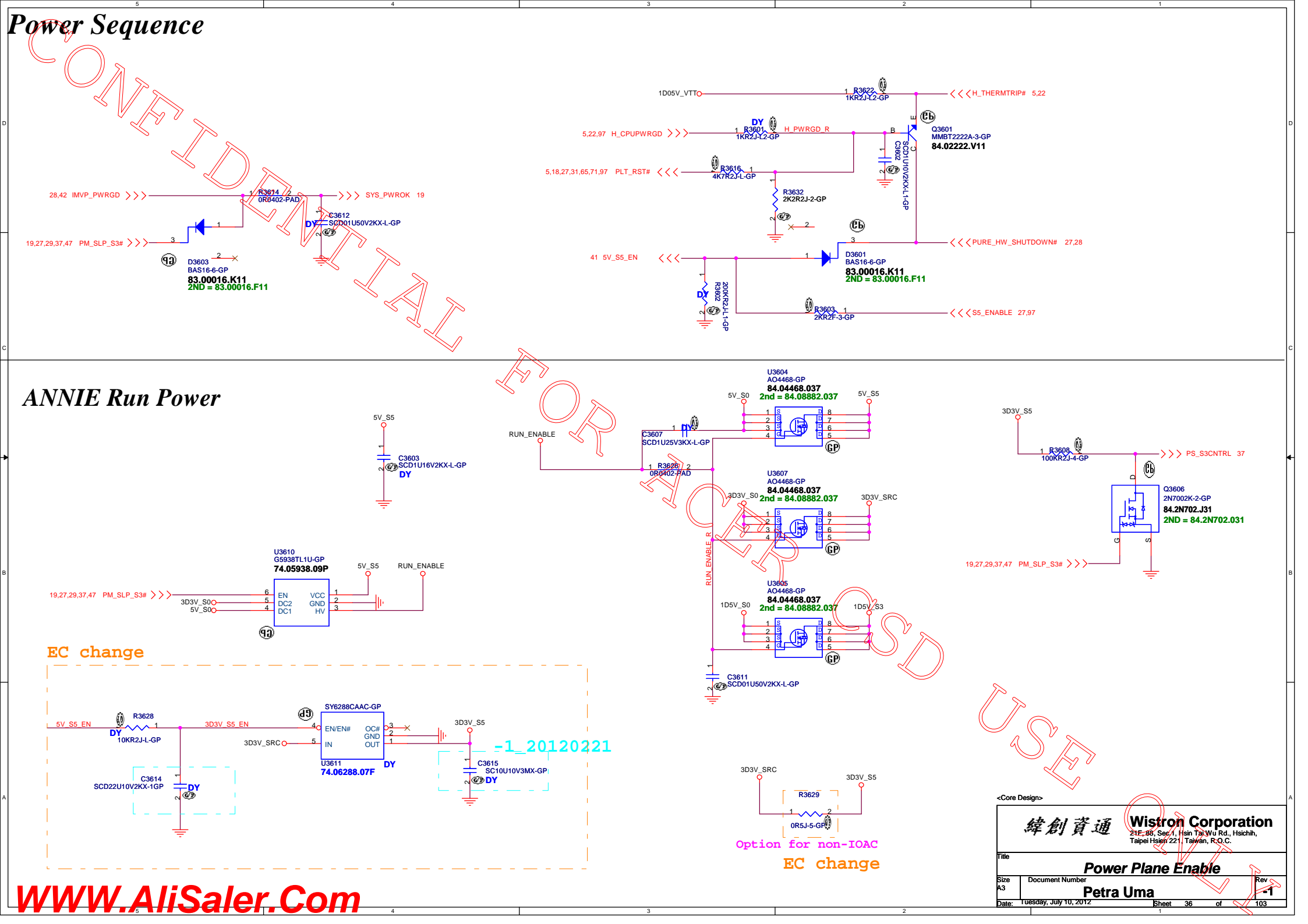
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	Petra Uma		-1
Date:	Wednesday, February 22, 2012	Sheet 34 of	103

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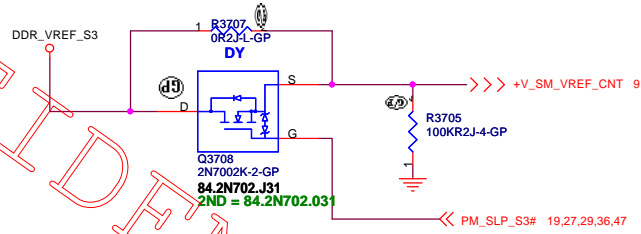
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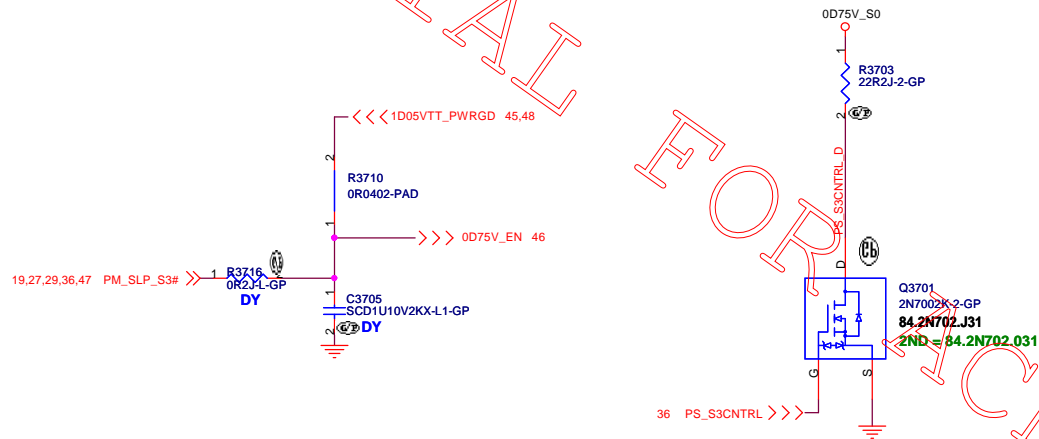
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>USB 3.0 Controller</div>		
Size <div>A4</div>	Document Number <div>Petra Uma</div>	Rev <div>-1</div>
Date: Wednesday, February 22, 2012		Sheet 35 of 103



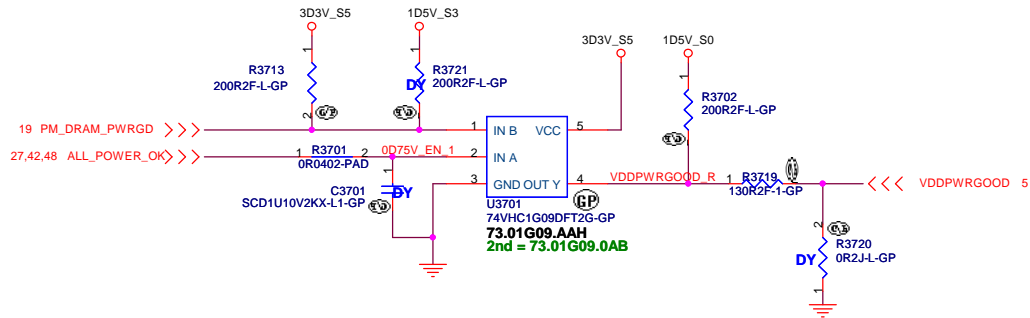
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



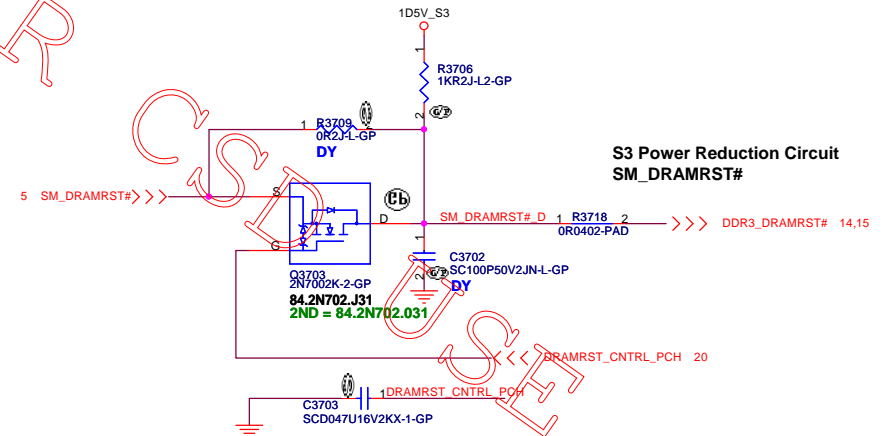
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

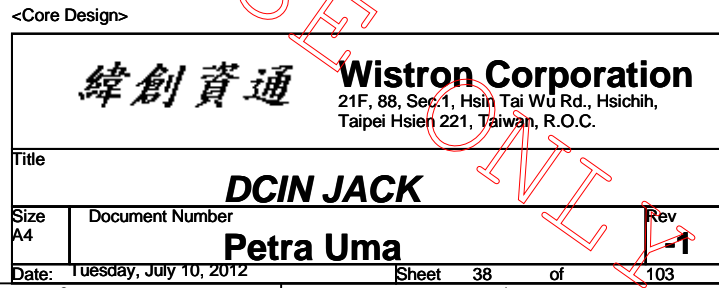


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

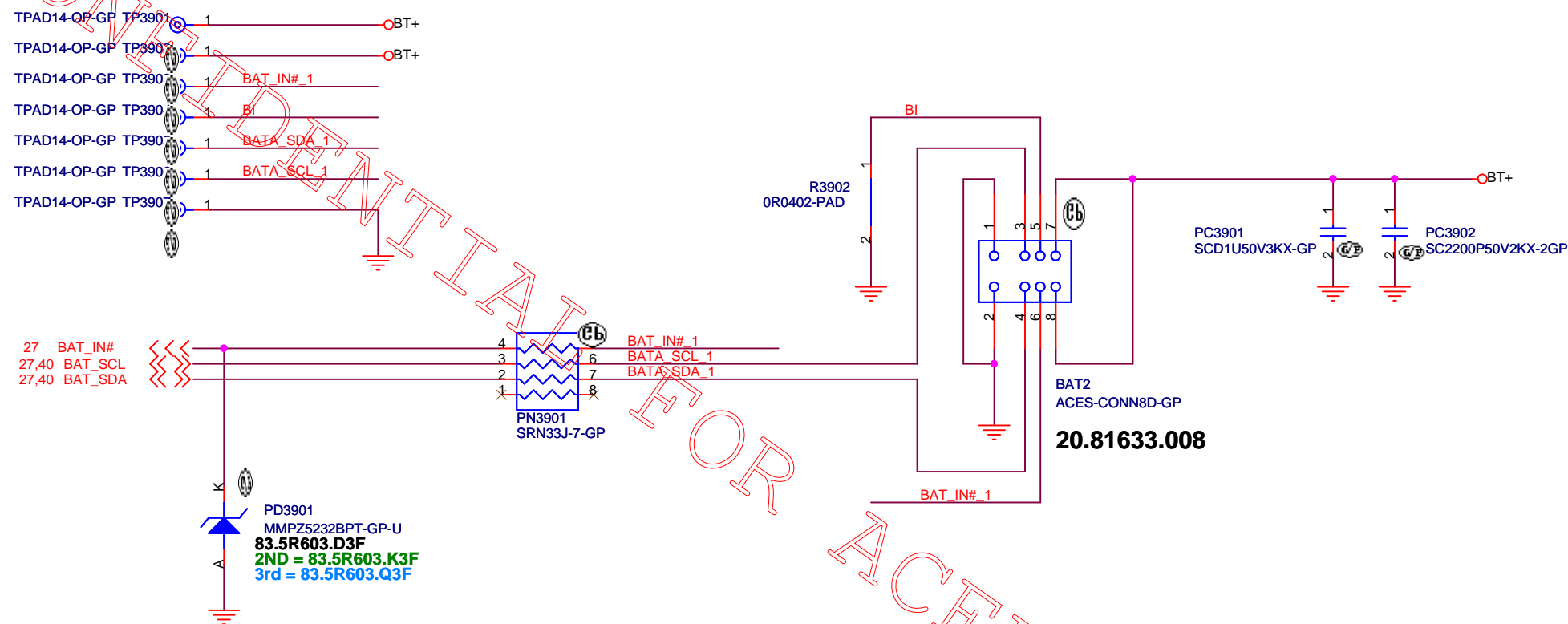


S3 Power Reduction Circuit
SM_DRAMPST#

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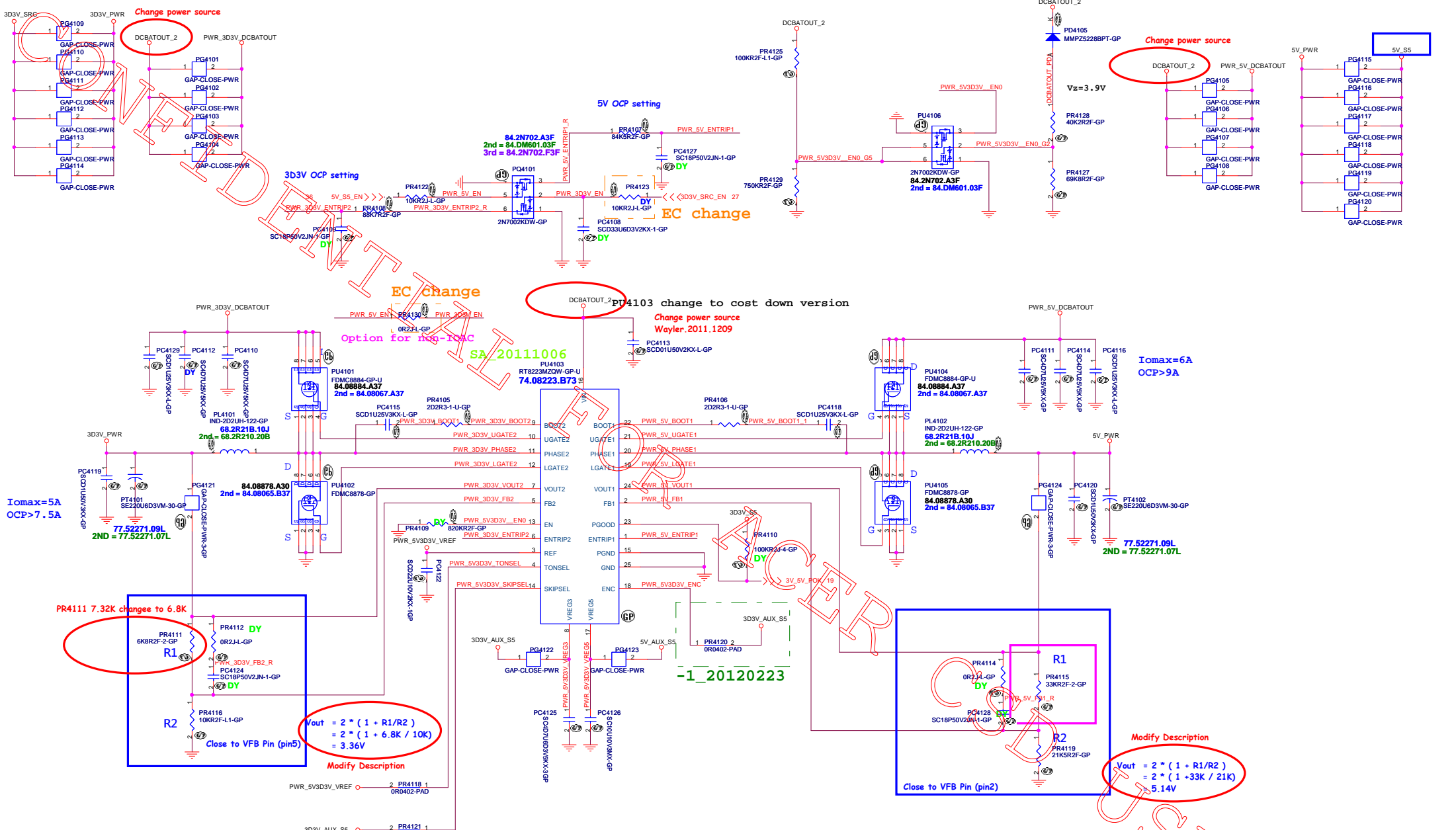


BATTERY CONNECTOR



<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BATT CONN			
Size	Document Number		Rev
A4	Petra Uma		-1
Date: Tuesday, July 10, 2012		Sheet	39 of 103



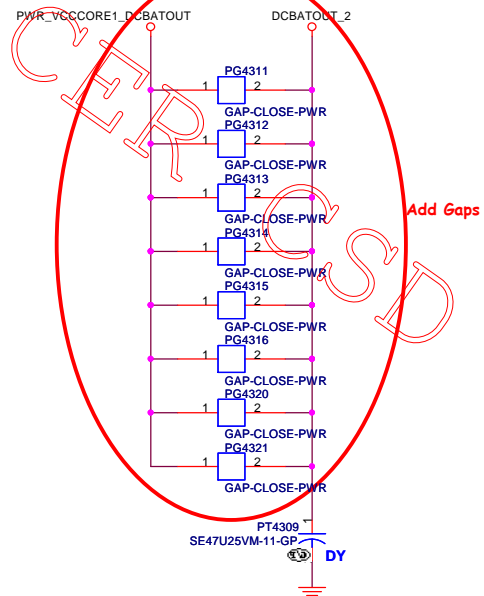
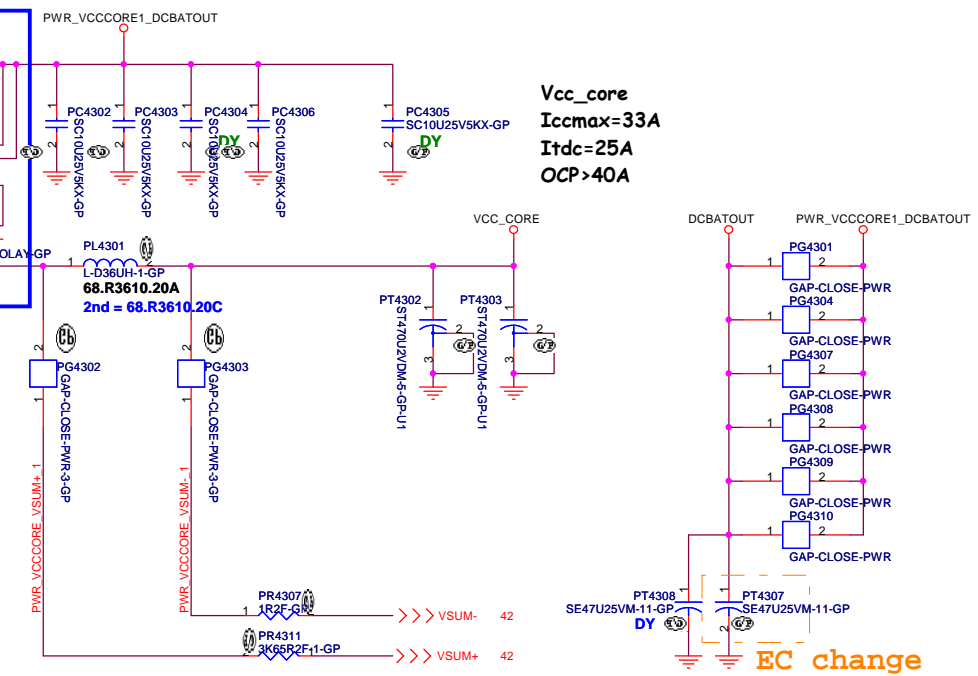
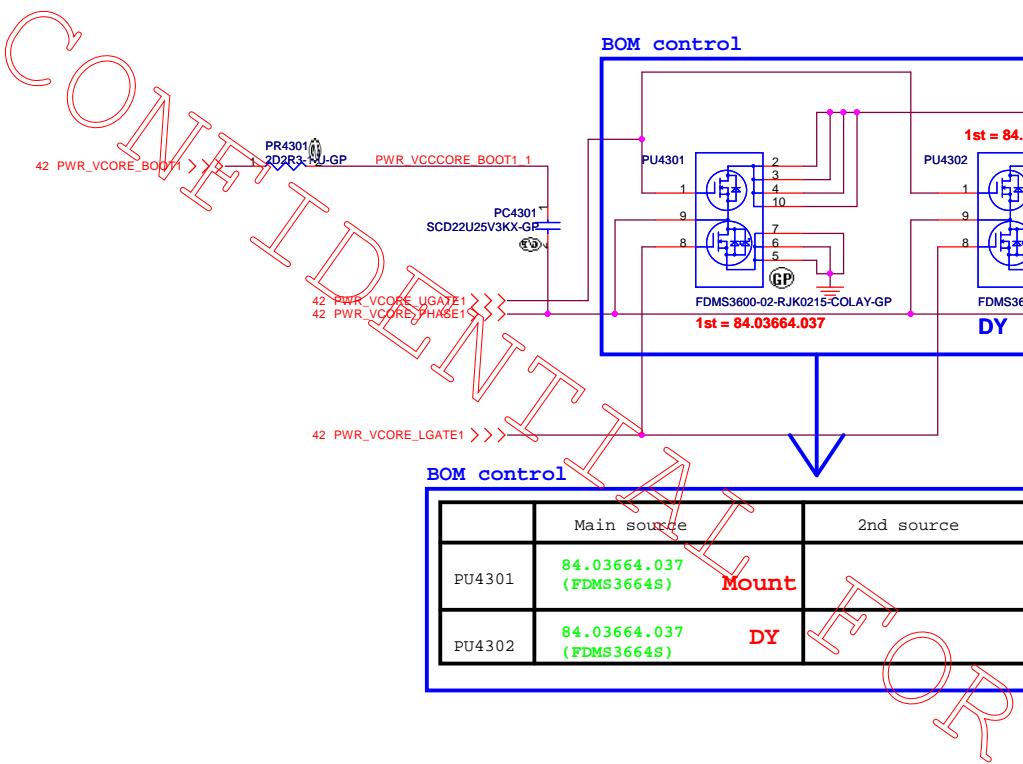
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

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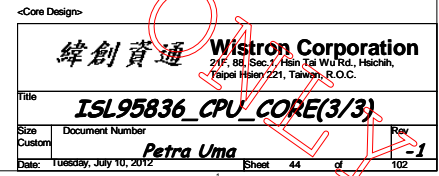


Title				ISL95836_CPU_CORE(1/3)			
Size		Document Number				Rev	
Custom		Petra Uma				-	
Date:		Tuesday, July 10, 2012		Sheet 42		of 102	

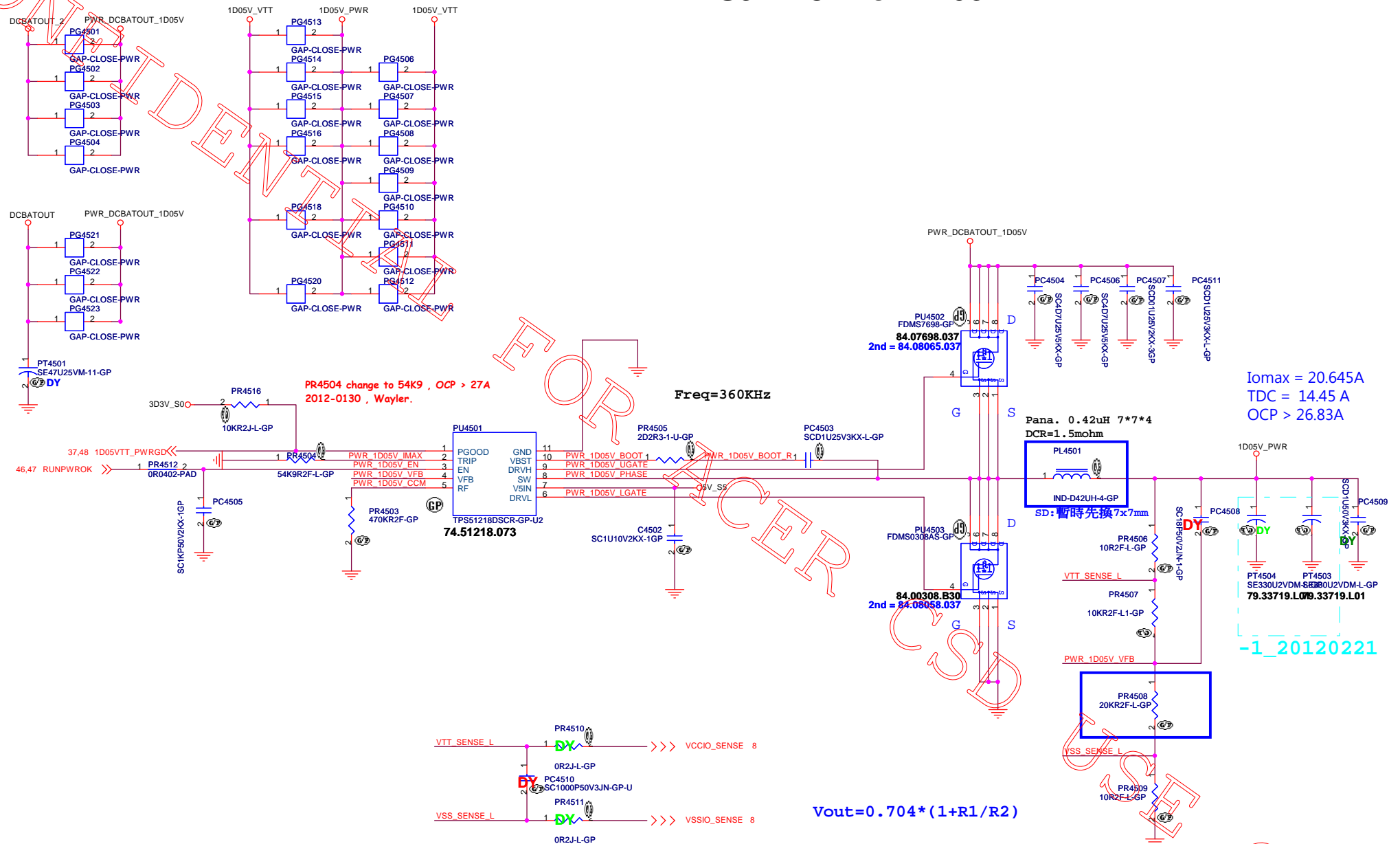


USE

USE



TPS51218D for 1D05V



<Core Design>

緯創資通

Wistron Corporation
21F-88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DC to DC 1D05V(TPS51218D)

Size

A3

Date: Tuesday, July 10, 2012

Petra Uma

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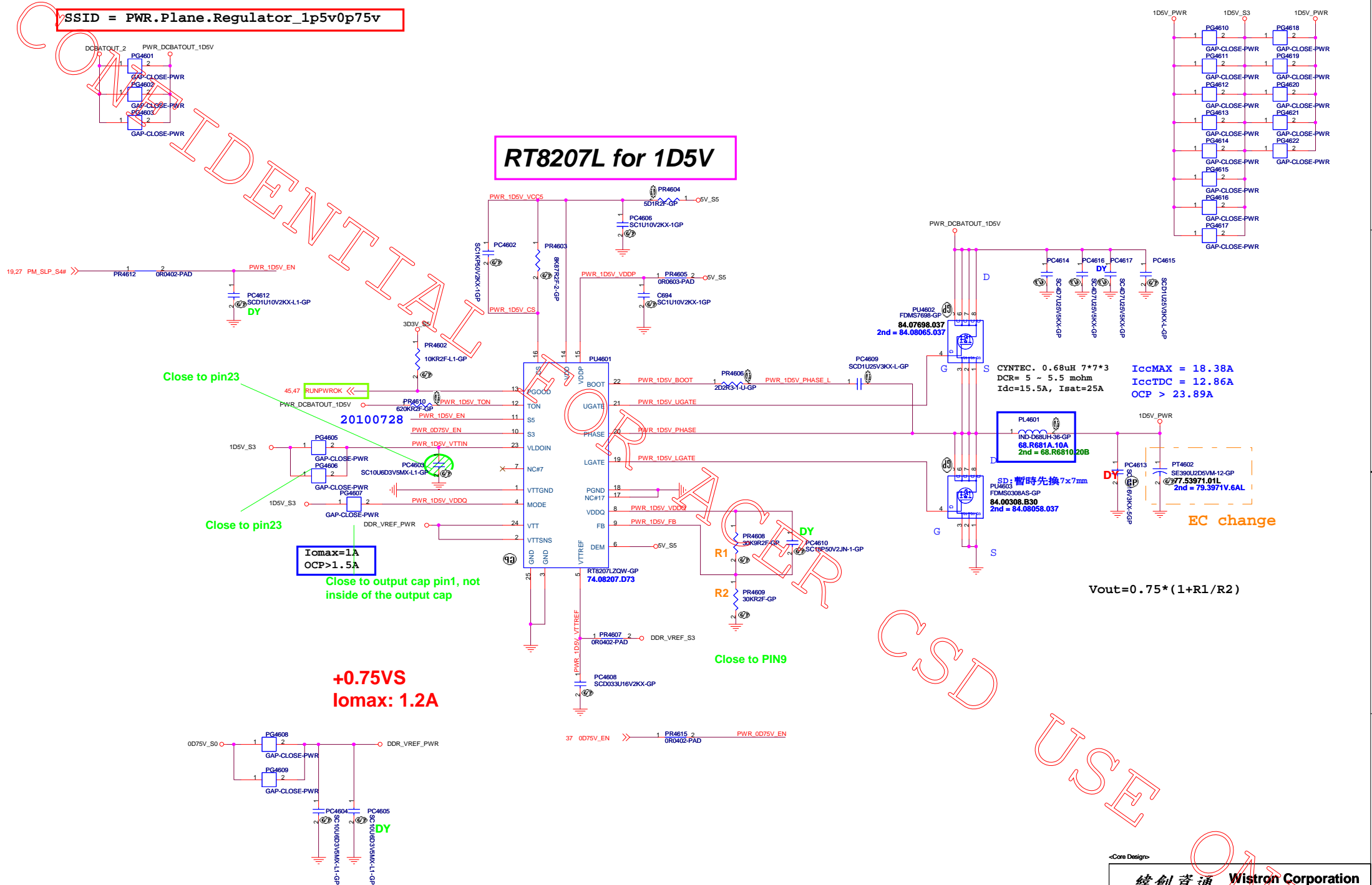
Rev

-1

103

SSID = PWR.Plane.Regulator_lp5v0p75v

RT8207L for 1D5V



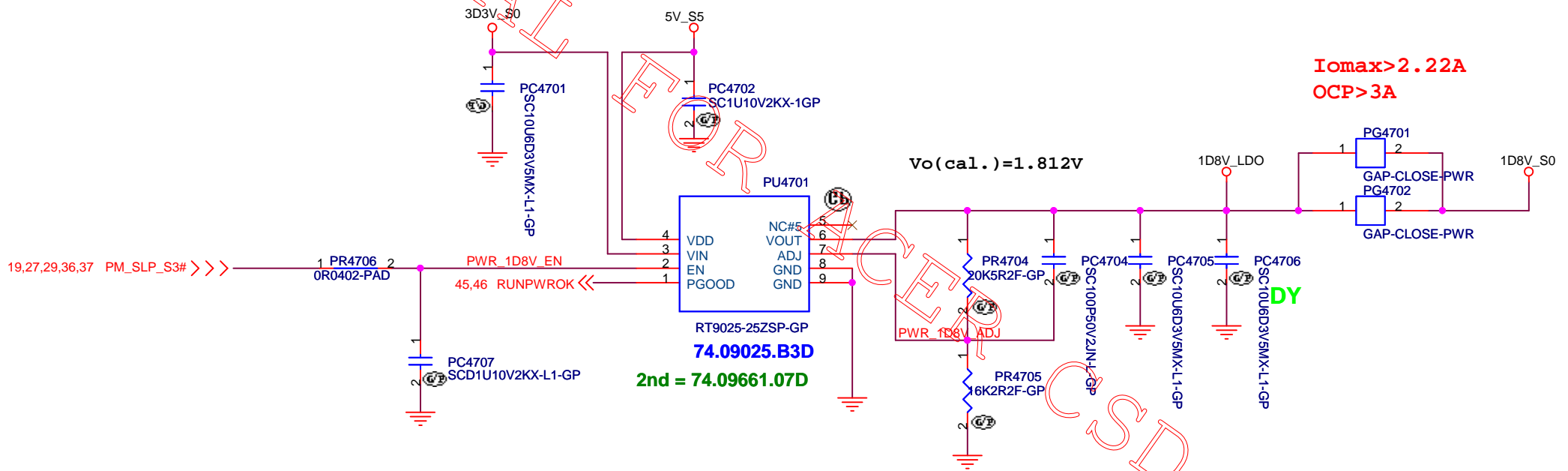
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緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taiwan 300, R.O.C.

Title		RT8207	
Size	Document Number	Rev	
Custom		Petra Uma	
Date:	Tuesday, July 10, 2012	Sheet	46 of 103

SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LDO 1D8V(RT9025)

Size
A4

Document Number

Petra Uma

Rev

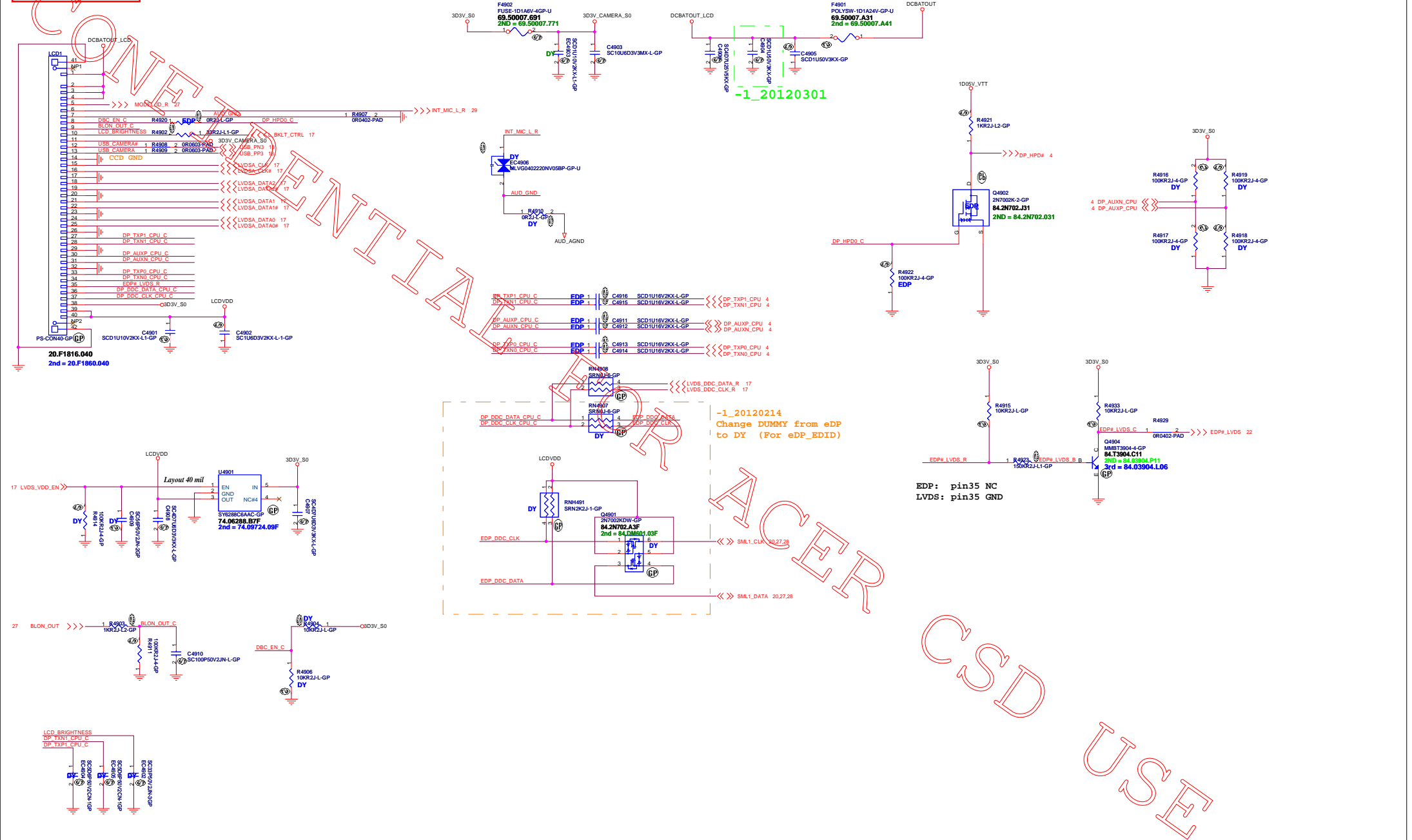
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Date: Tuesday, July 10, 2012

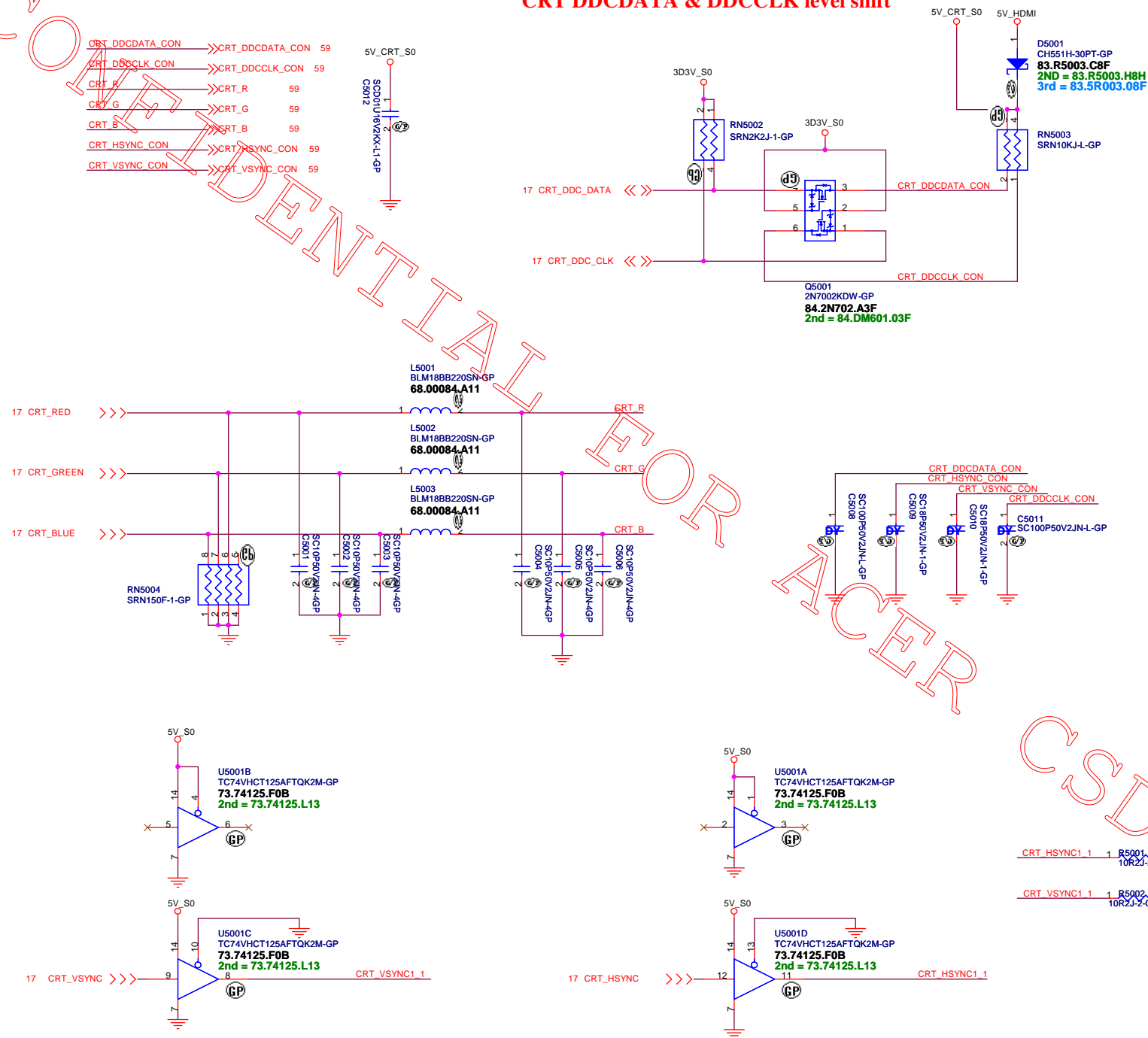
Sheet 47 of 103

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SSID = VIDEO



CRT DDCDATA & DDCCLK level shift



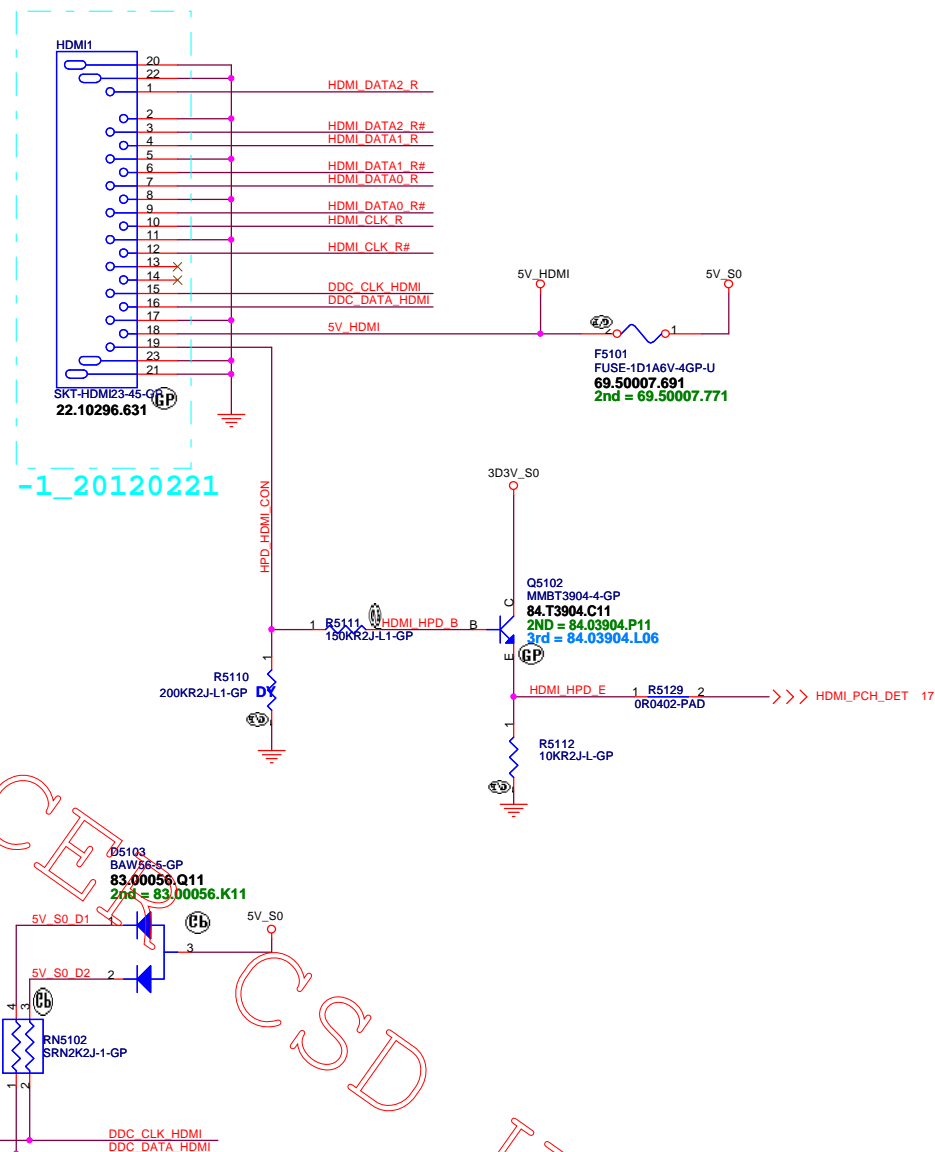
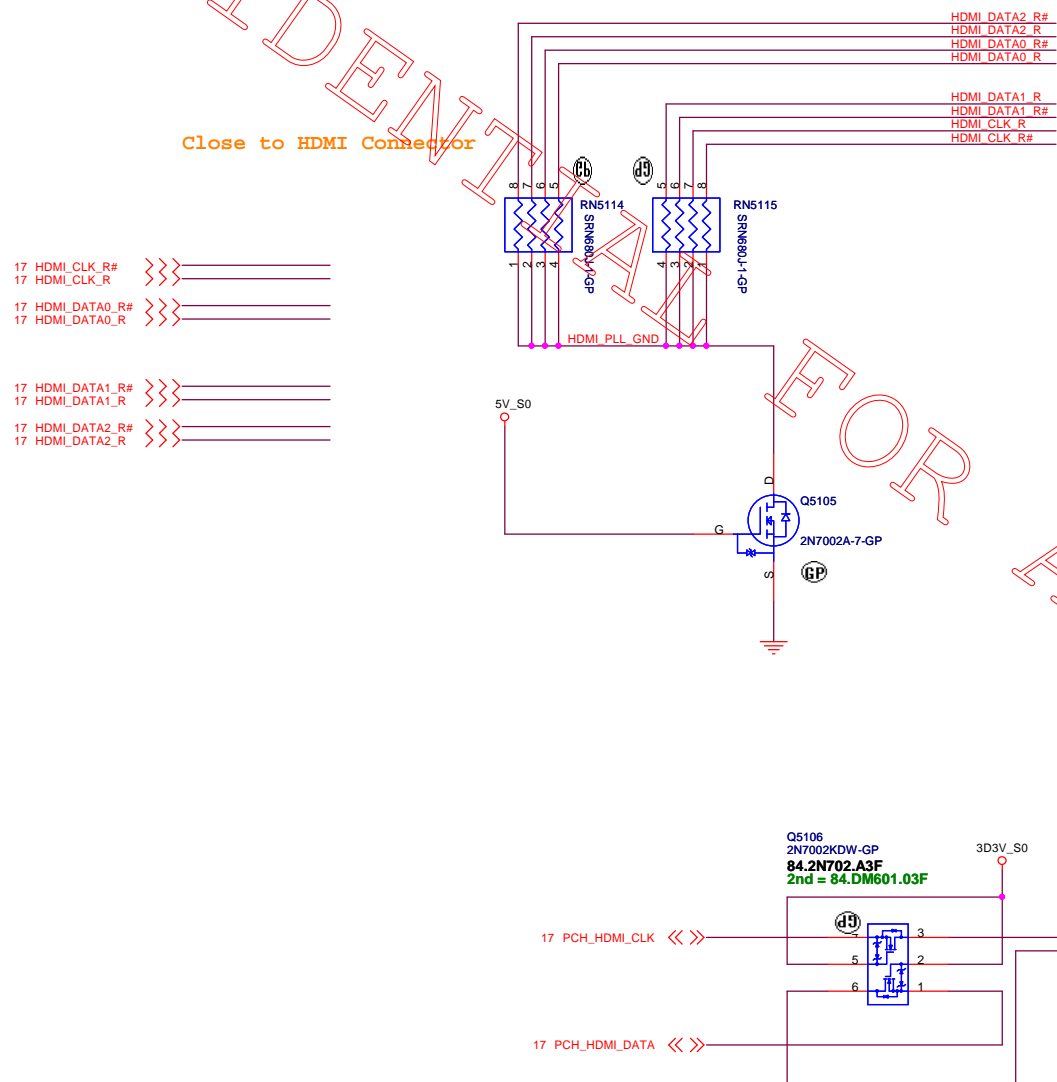
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緯創資通 Wistron Corporation
21E, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsin 221, Taiwan, R.O.C.

Title		CRT Connector	
Size A3	Document Number	Petra Uma	
Date: Tuesday, July 10, 2012	Sheet 50	of 103	Rev -1

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



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緯創資通

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HDMI Level Shifter/Connector

Size

Document Number

Petra Uma

Date: Tuesday, July 10, 2012

Sheet

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1	
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of

11

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LED BACKLIGHT CONVERTER POWER

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

eDP

Size

A4

Document Number

Petra Uma

Rev

-1

Date: Wednesday, February 22, 2012

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

S-VIDEO

Size
A4

Document Number

Petra Uma

Rev
-1

Date: Wednesday, February 22, 2012

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<Core Design>

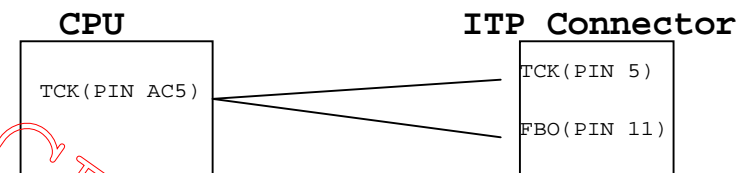
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Title		
Reserved		
Size	Document Number	Rev
A4	Petra Uma	-1
Date: Wednesday, February 22, 2012		Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

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緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

ITP

Size
A4

Document Number

Petra Uma

Rev
-1

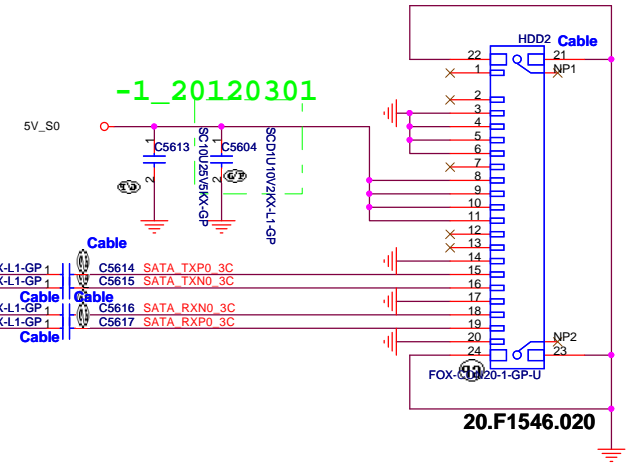
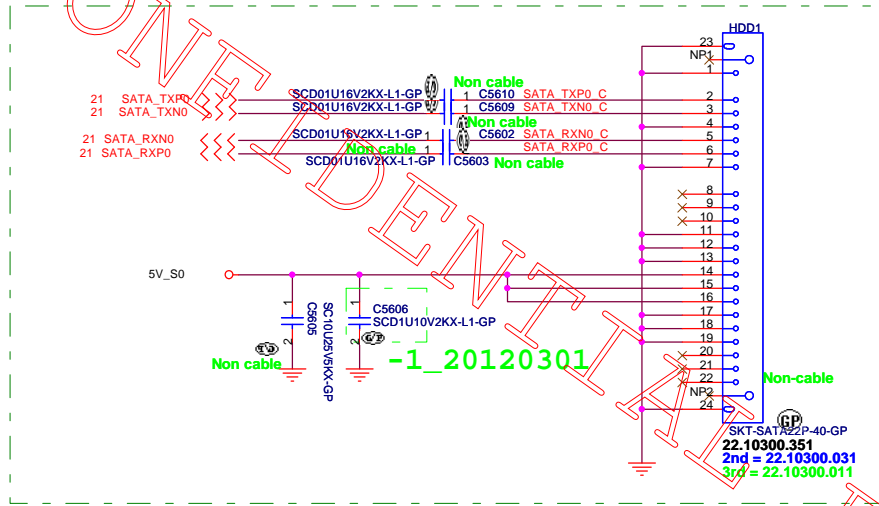
Date: Wednesday, February 22, 2012

Sheet 55 of 103

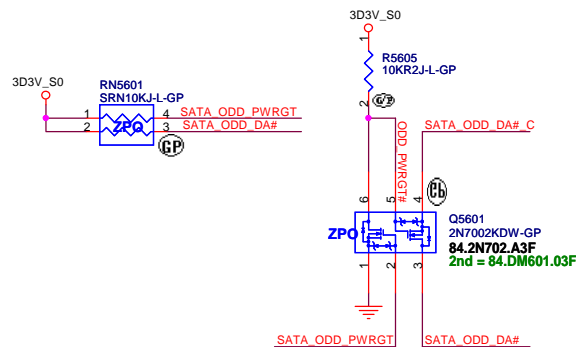
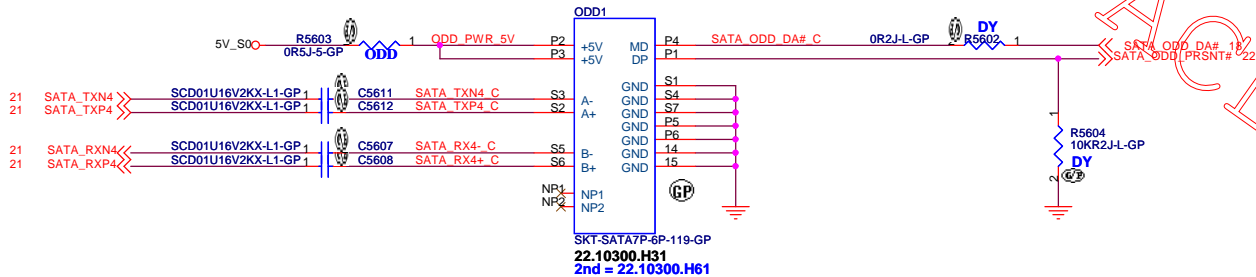
SSID = SATA

SATA HDD Connector

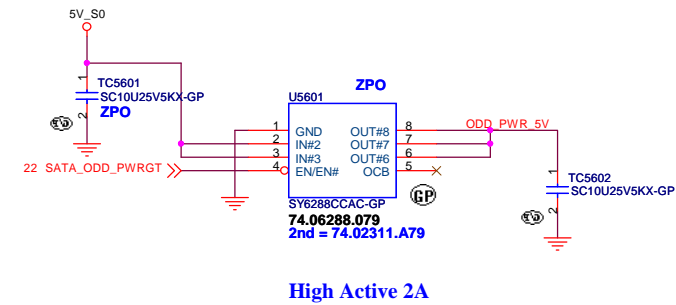
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ODD Connector



SATA Zero Power ODD



High Active 2A

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Wistron Corporation
21F, 88, Sec.1, Hsui Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD/ODD

Size

Document Number

Petra Uma

Rev

-1

Date: Tuesday, July 10, 2012

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ESATA Power

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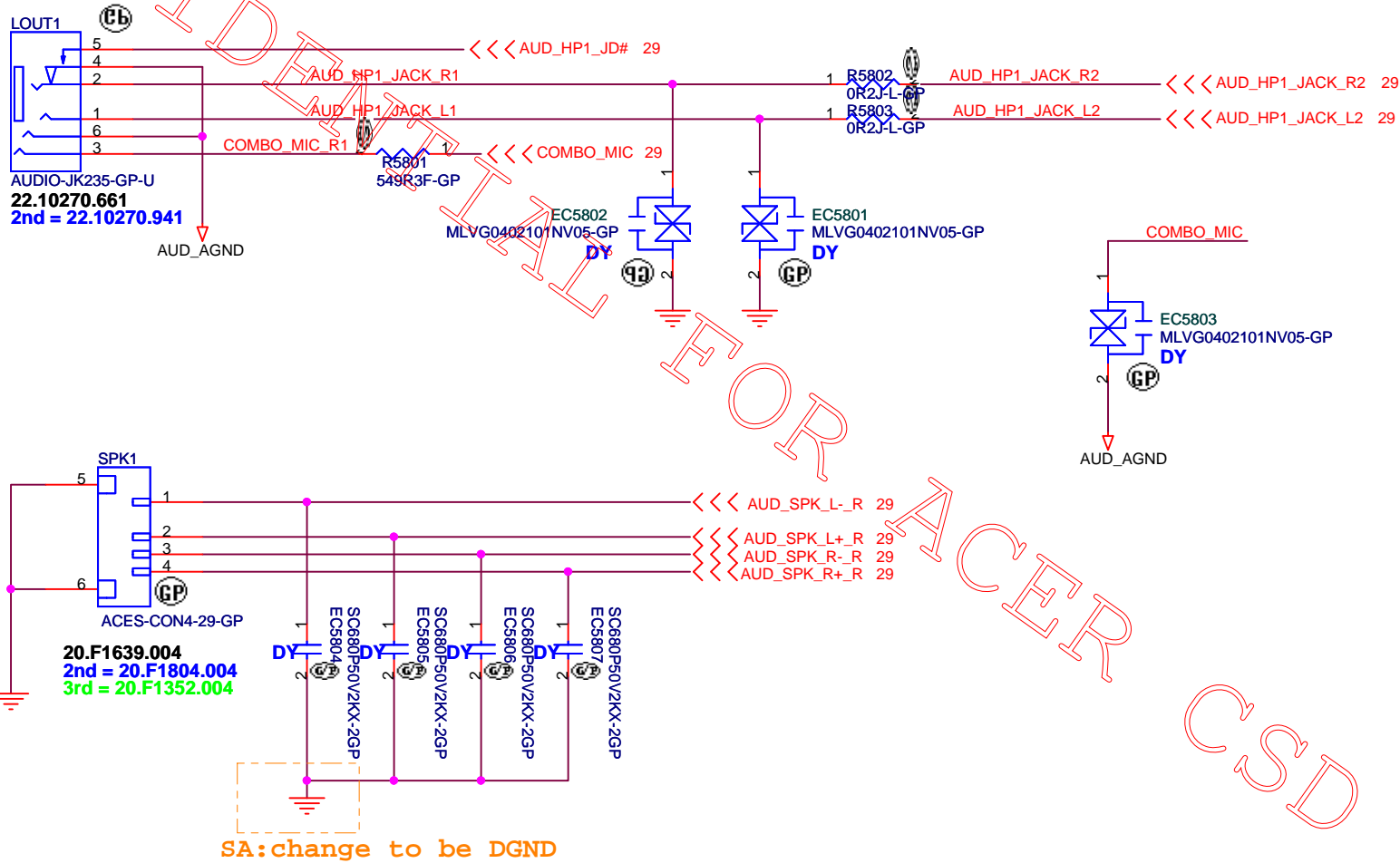
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title E-SATA/USB CHARGER

Size A4 Document Number Petra Uma Rev -1

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SSID = AUDIO



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio Jack

Size
A4

Document Number

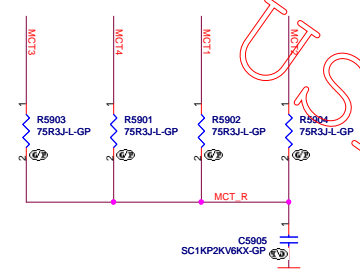
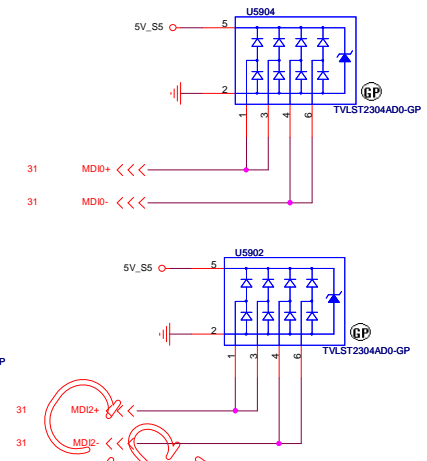
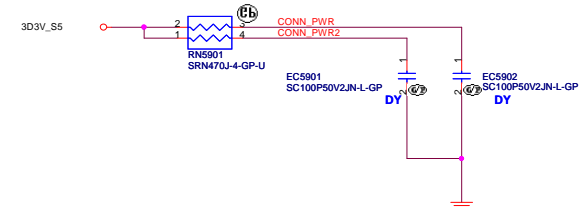
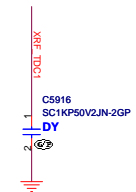
Petra Uma

Rev
-1

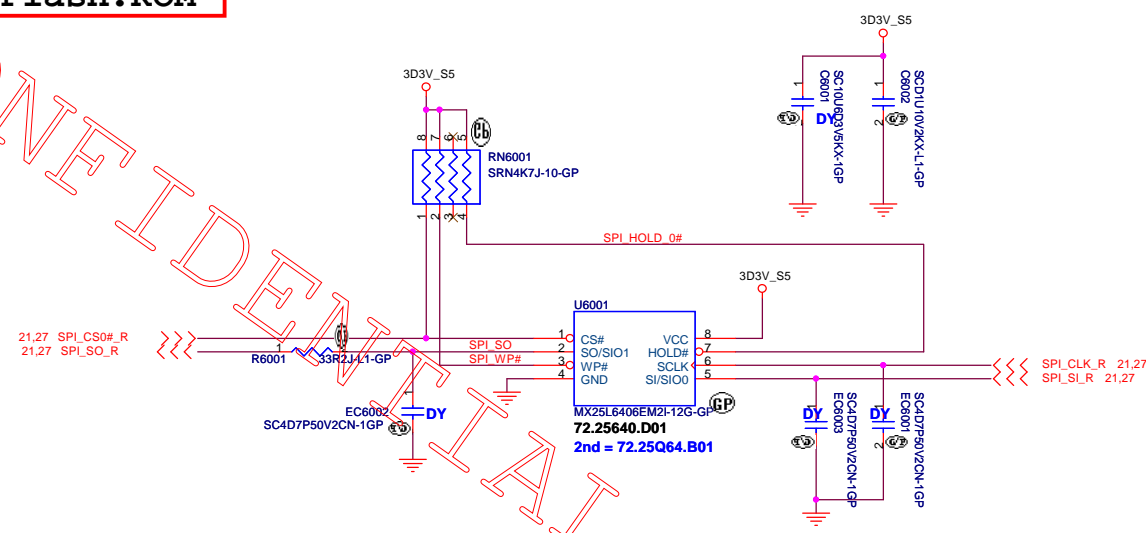
Date: Tuesday, July 10, 2012

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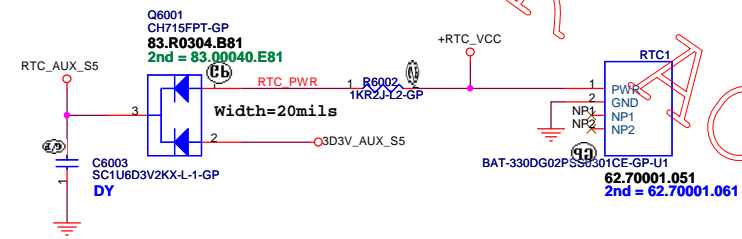
SSID = LAN



SSID = Flash.ROM

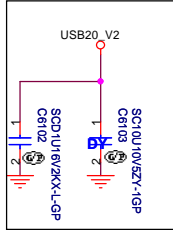


SSID = RTC



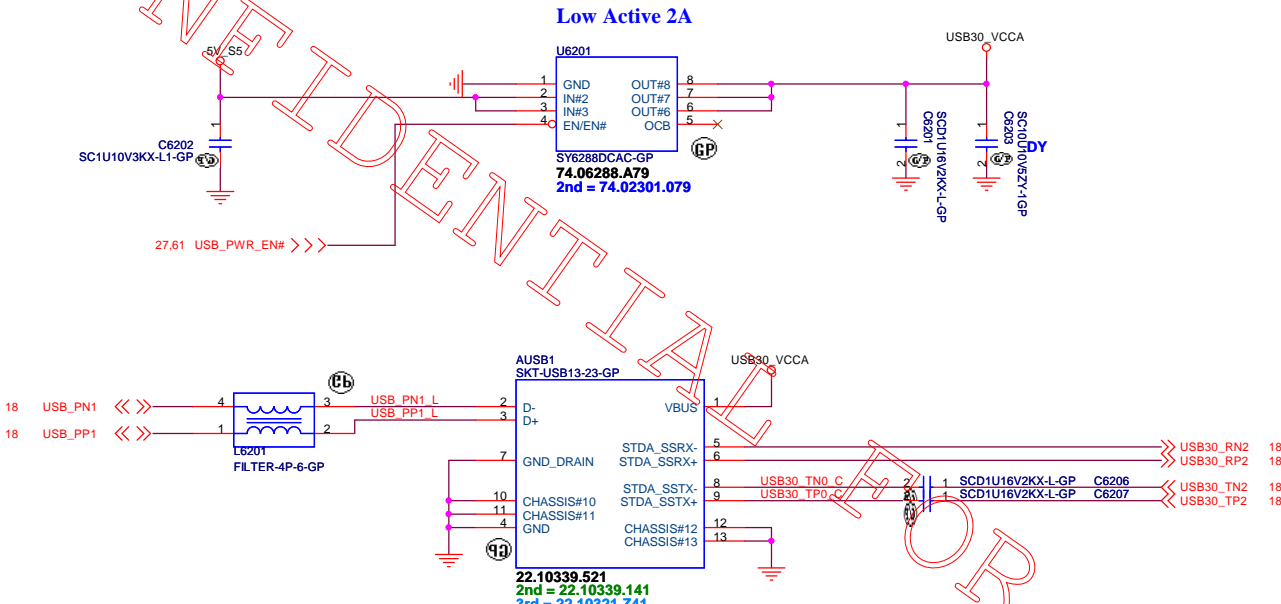
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		Flash/RTC	
Size	Document Number	Rev	
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~~SSID~~ = USB



Close to AUSB2

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USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module

(Blanking)

<Core Design>

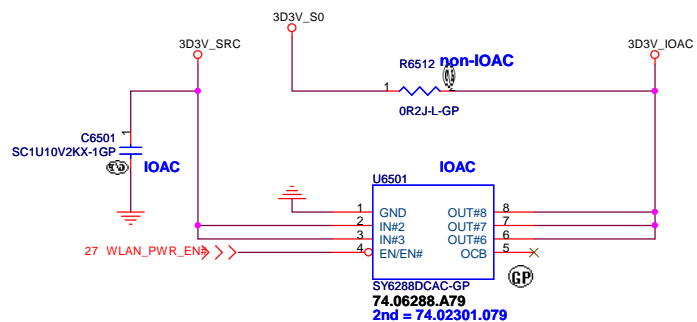
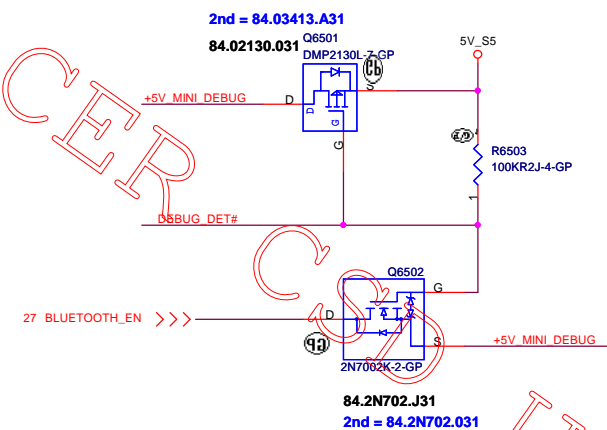
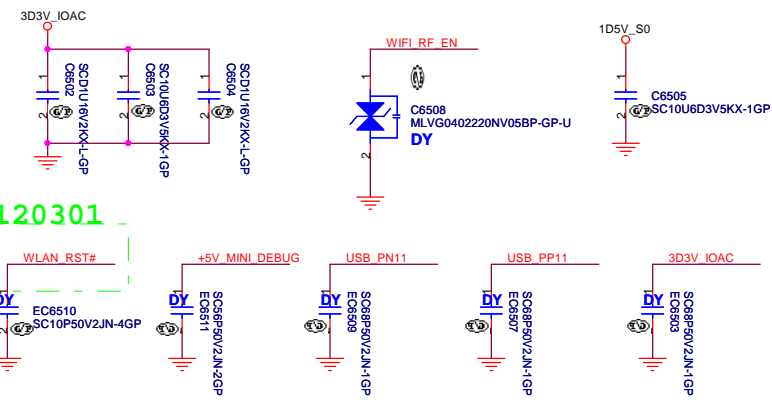
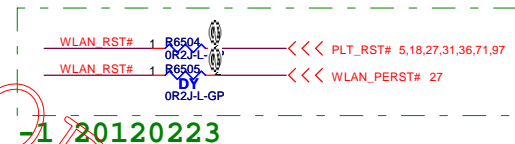
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Title <div>Bluetooth</div>		
Size <div>A4</div>	Document Number <div>Petra Uma</div>	Rev <div>-1</div>
Date: Wednesday, February 22, 2012		Sheet 63 of 103

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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
RESERVED		
Size	Document Number	Rev
A4	Petra Uma	-1
Date: Wednesday, February 22, 2012		Sheet 64 of 103

Mini Card Connector(802.11a/b/g/n)



SSID = Wireless

Mini Card Connector(WWAN)

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緯創資通

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Title

WWAN Connector

Size

A4

Document Number

Petra Uma

Rev

-1

Date: Wednesday, February 22, 2012

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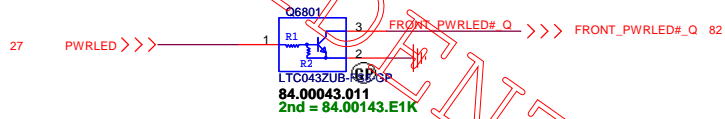
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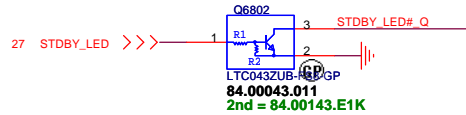
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Petra Uma</div>	Rev <div>-1</div>
Date: Wednesday, February 22, 2012		Sheet 67 of 103

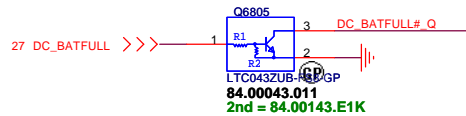
Power button LED



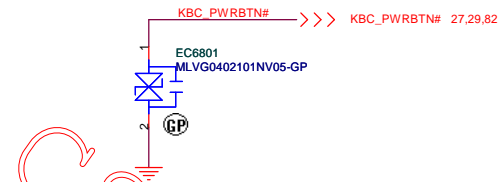
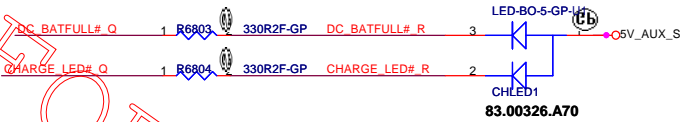
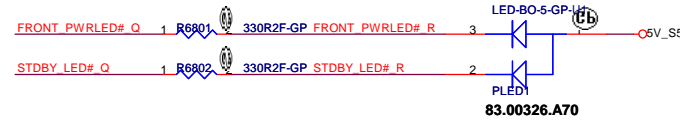
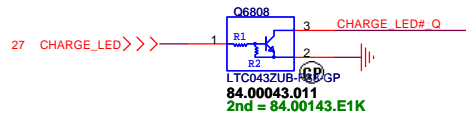
Power STDBY_LED



Battery LED2(DC_BATFULL)

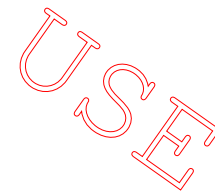
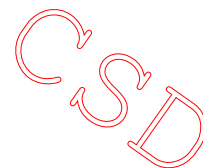
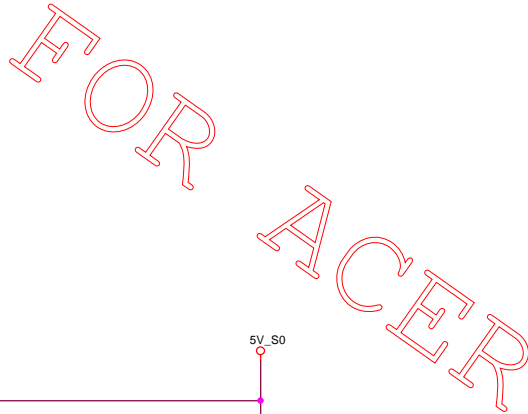


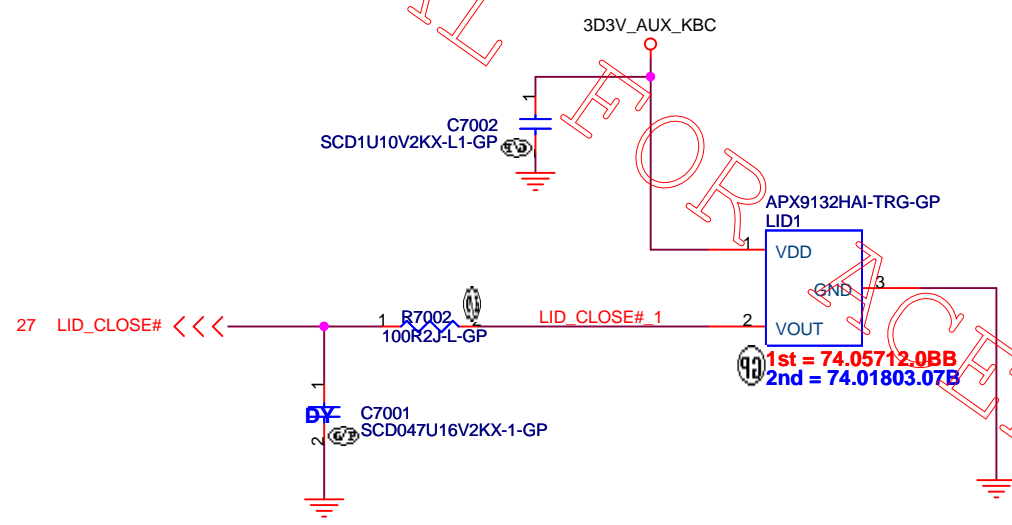
Battery LED1(CHARGE)



<Core Design>			
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LED Bard/Power Button			
Size	Document Number		Rev
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Internal KeyBoard Connector





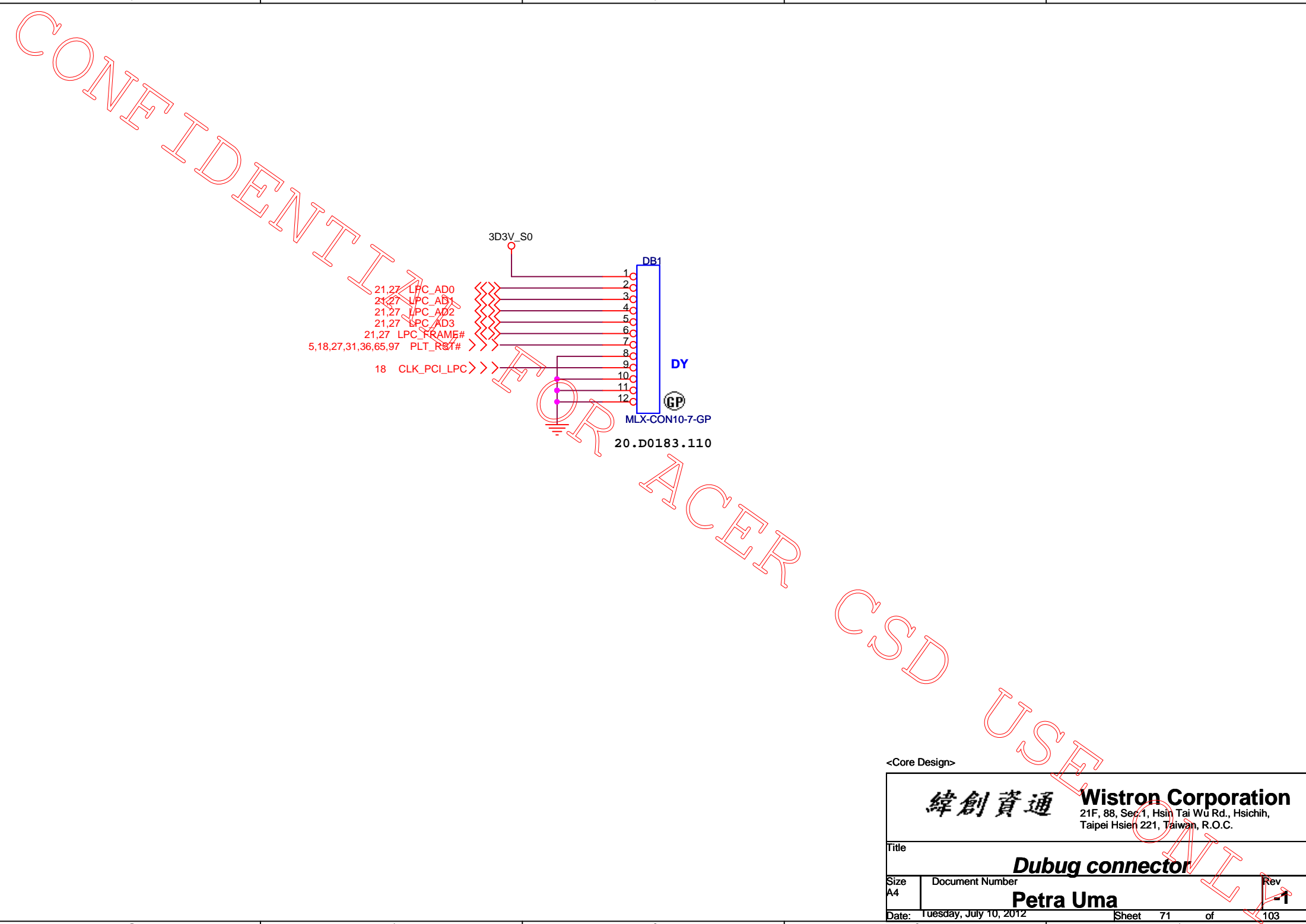
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Wistron Corporation
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Title			Hall Sensor	
Size A4	Document Number		Petra Uma	
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Dubug connector		
Size	Document Number	Rev
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Title

Reserved

Size
A4

Document Number

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-1

Date: Wednesday, February 22, 2012

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Title

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Rev

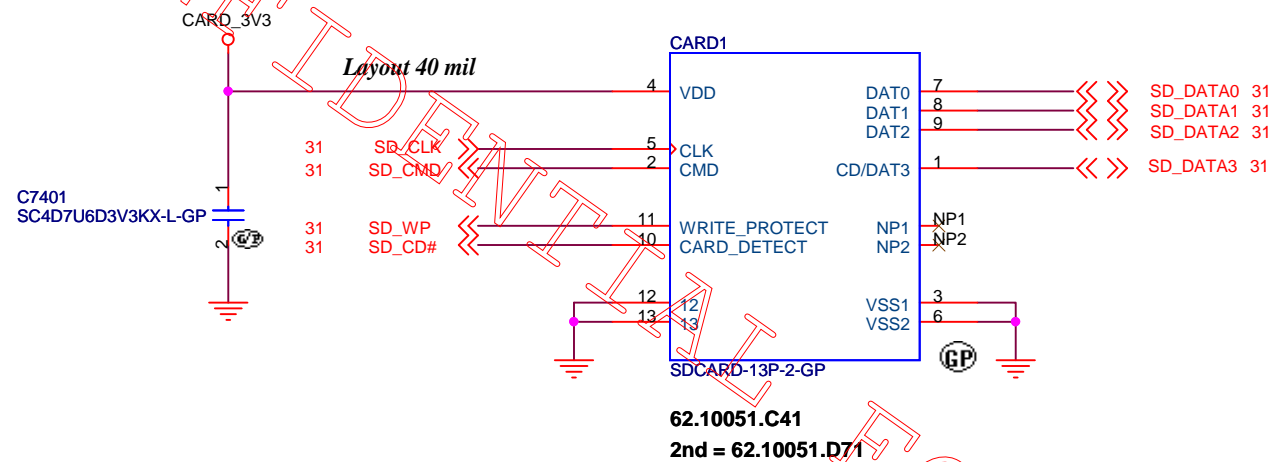
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Date: Wednesday, February 22, 2012

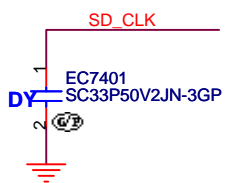
Sheet 73 of 103

SSID = SDIO

SD/MMC Card Reader



BCM57765/BCM57785 Pin Number	Signal Name	SD/MMC Interface	MS-Pro Interface	xD Interface
21	CR_CLK/RX_BY#	CR_CLK	MS_CLK	RX_BY#
26	CR_CMD/CLE	CR_CMD	MS_BS	CLE
25	CR_DATA0	CR_DATA0	MS_DATA0	XD_DATA0
24	CR_DATA1	CR_DATA1	MS_DATA1	XD_DATA1
23	CR_DATA2	CR_DATA2	MS_DATA2	XD_DATA2
22	CR_DATA3	CR_DATA3	MS_DATA3	XD_DATA3
52	CR_DATA4	CR_DATA4	MS_DATA4	XD_DATA4
53	CR_DATA5	CR_DATA5	MS_DATA5	XD_DATA5
54	CR_DATA6	CR_DATA6	MS_DATA6	XD_DATA6
55	CR_DATA7	CR_DATA7	MS_DATA7	XD_DATA7
60	ALE	-	-	ALE
1	SD_DETECT/WE#	CR_DETECT	-	WE#
9	RE#	-	-	RE#
59	CE#/MS_INS#	-	MS_INS#	CE#
57	CR_WP#/XD_WP# SD_WP#	-	-	WP#
68	XD_DETECT	-	-	XD_DETECT



<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CARD Reader CONN			
Size	Document Number	Rev	
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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

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<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

New Card

Size
A4

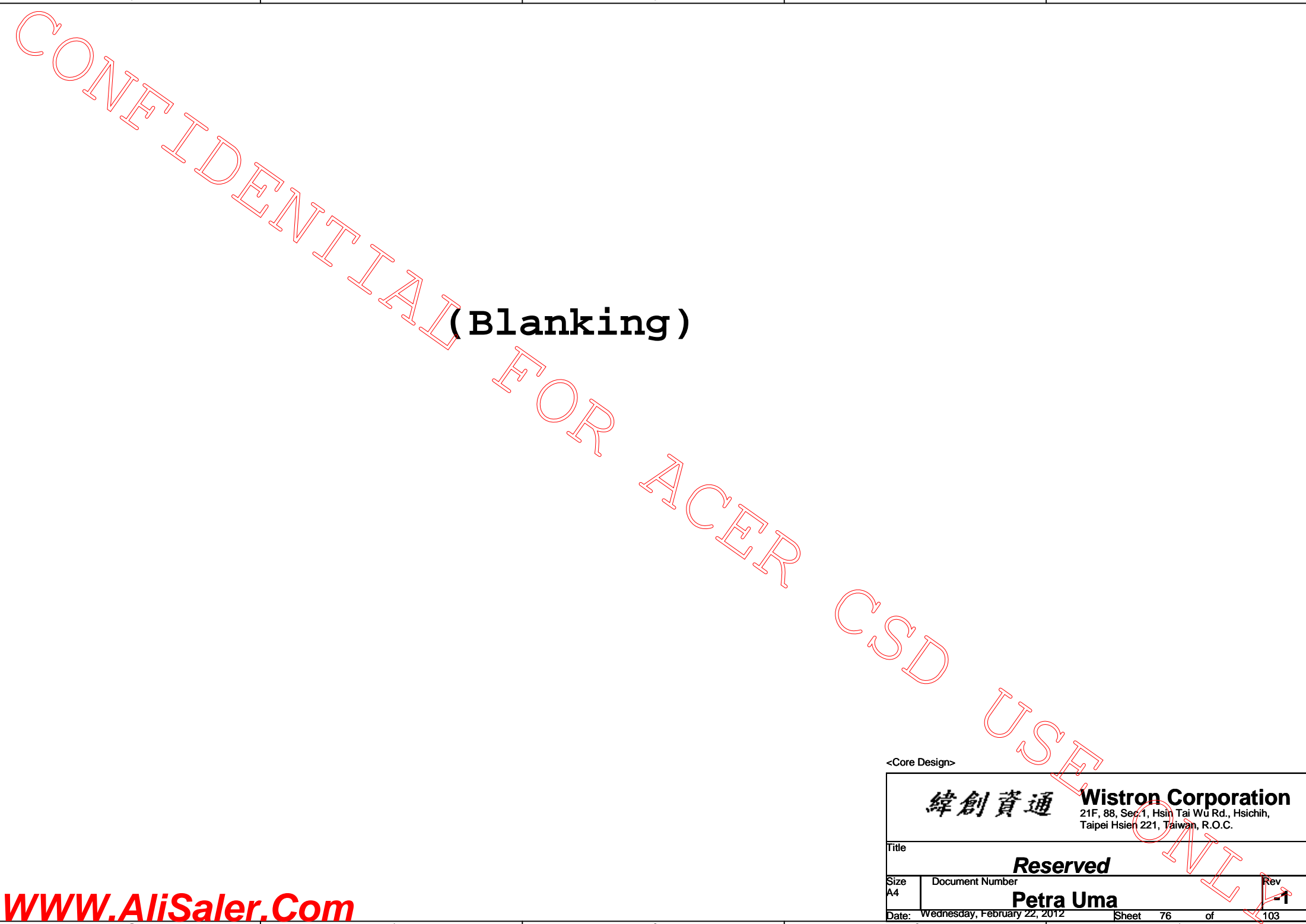
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Petra Uma

Rev
-1

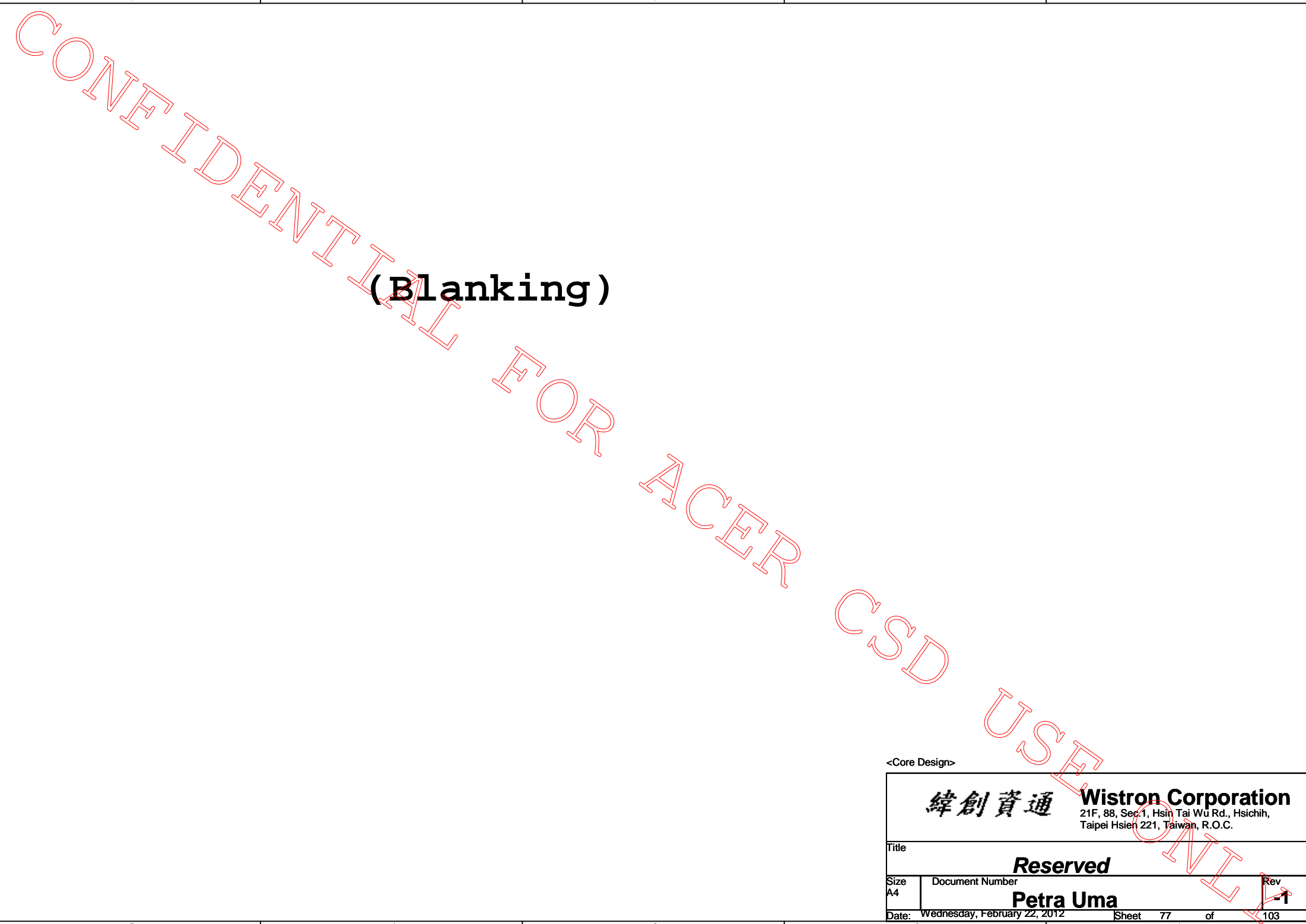
Date: Wednesday, February 22, 2012

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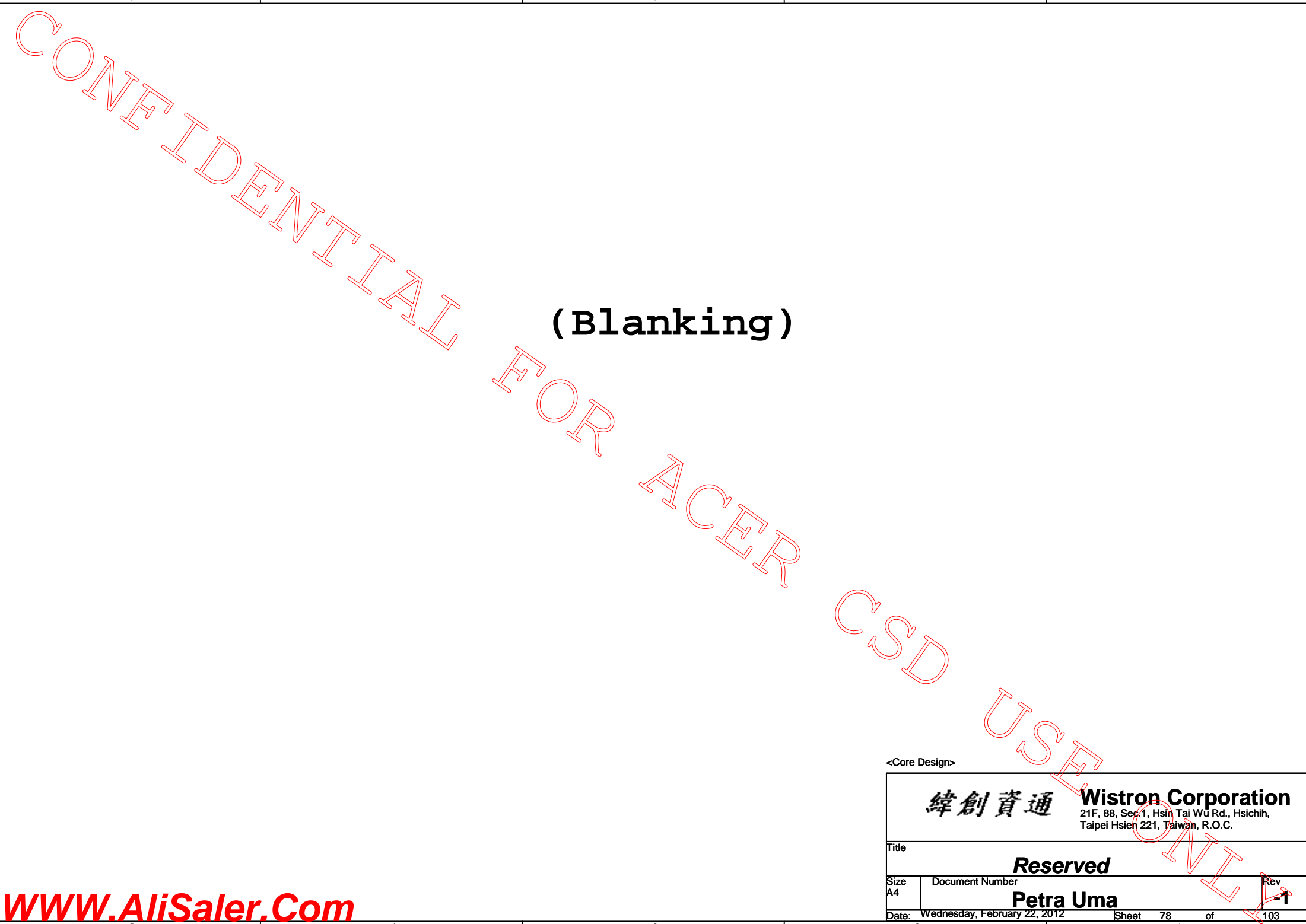
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number Petra Uma		Rev -1
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<Core Design>

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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Petra Uma</div>	Rev <div>-1</div>
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Title			
Reserved			
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Date:	Wednesday, February 22, 2012	Sheet 78 of	103

SSID = User.Interface

Free Fall Sensor

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Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

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Title

G- Sensor

Size
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Title

Reserved

Size
A4

Document Number

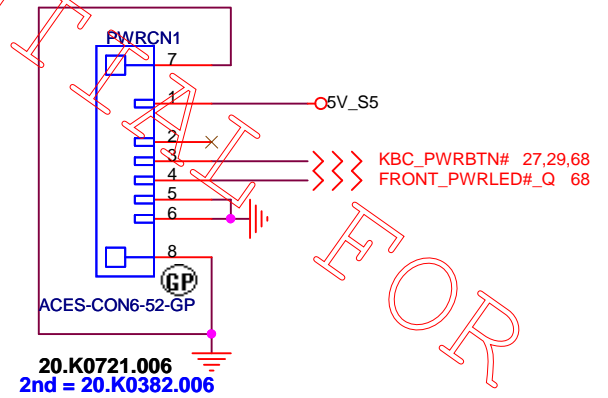
Petra Uma

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-1

Date: Wednesday, February 22, 2012

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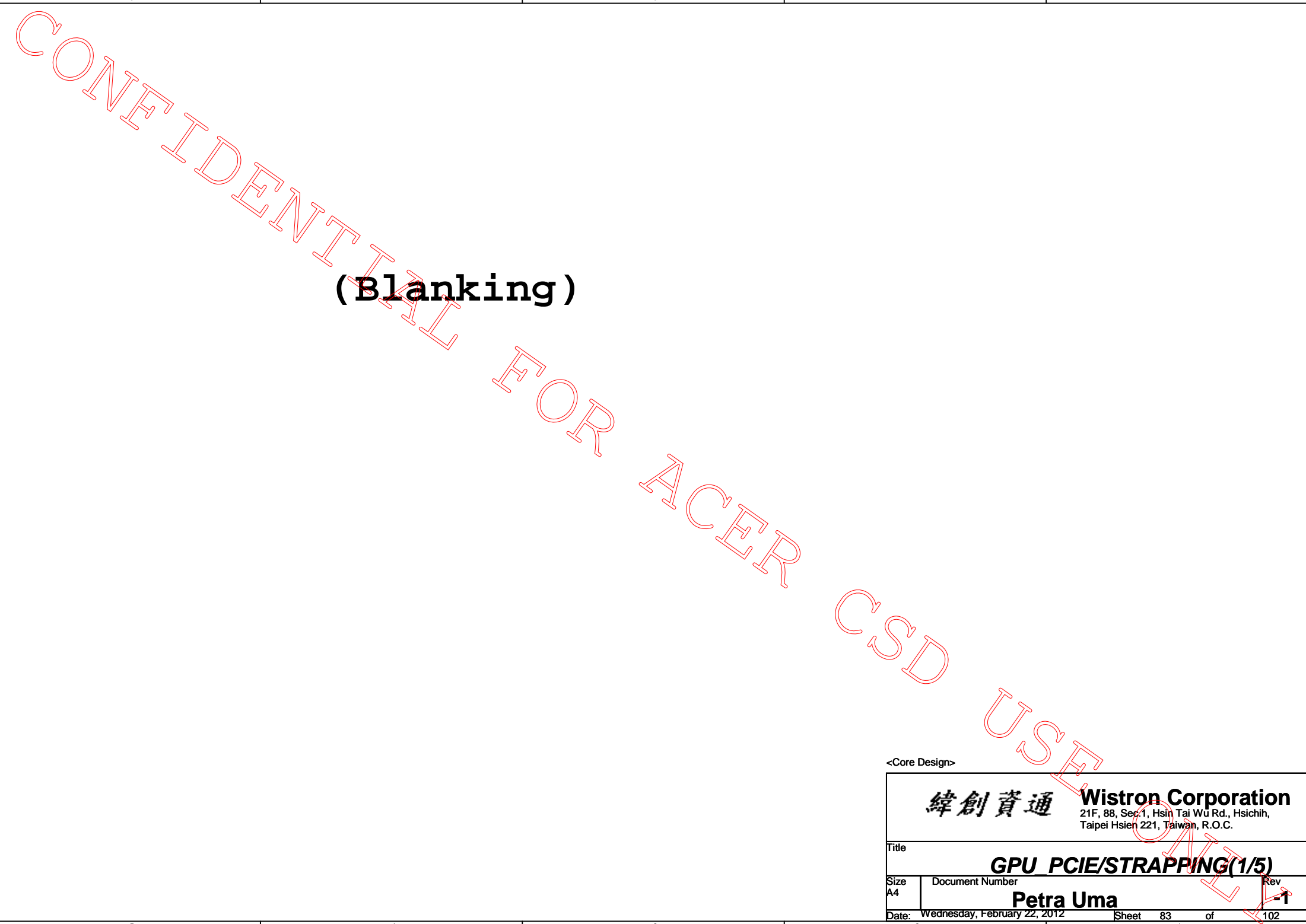
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

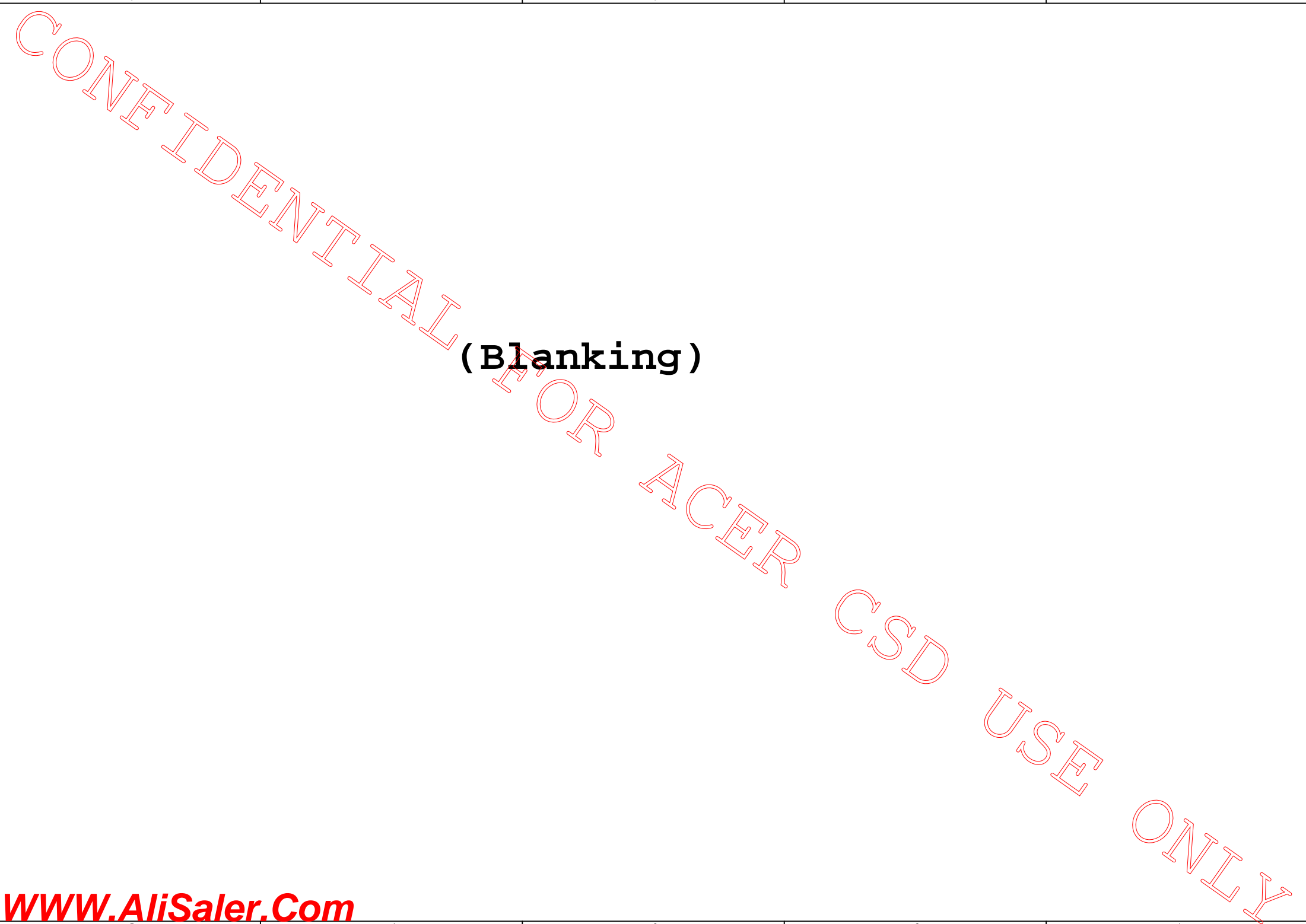
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Size	Document Number		Rev	
A4	Petra Uma		-1	
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<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
GPU PCIE/STRAPPING(1/5)		
Size	Document Number	Rev
A4	Petra Uma	-1
Date: Wednesday, February 22, 2012		Sheet 83 of 102

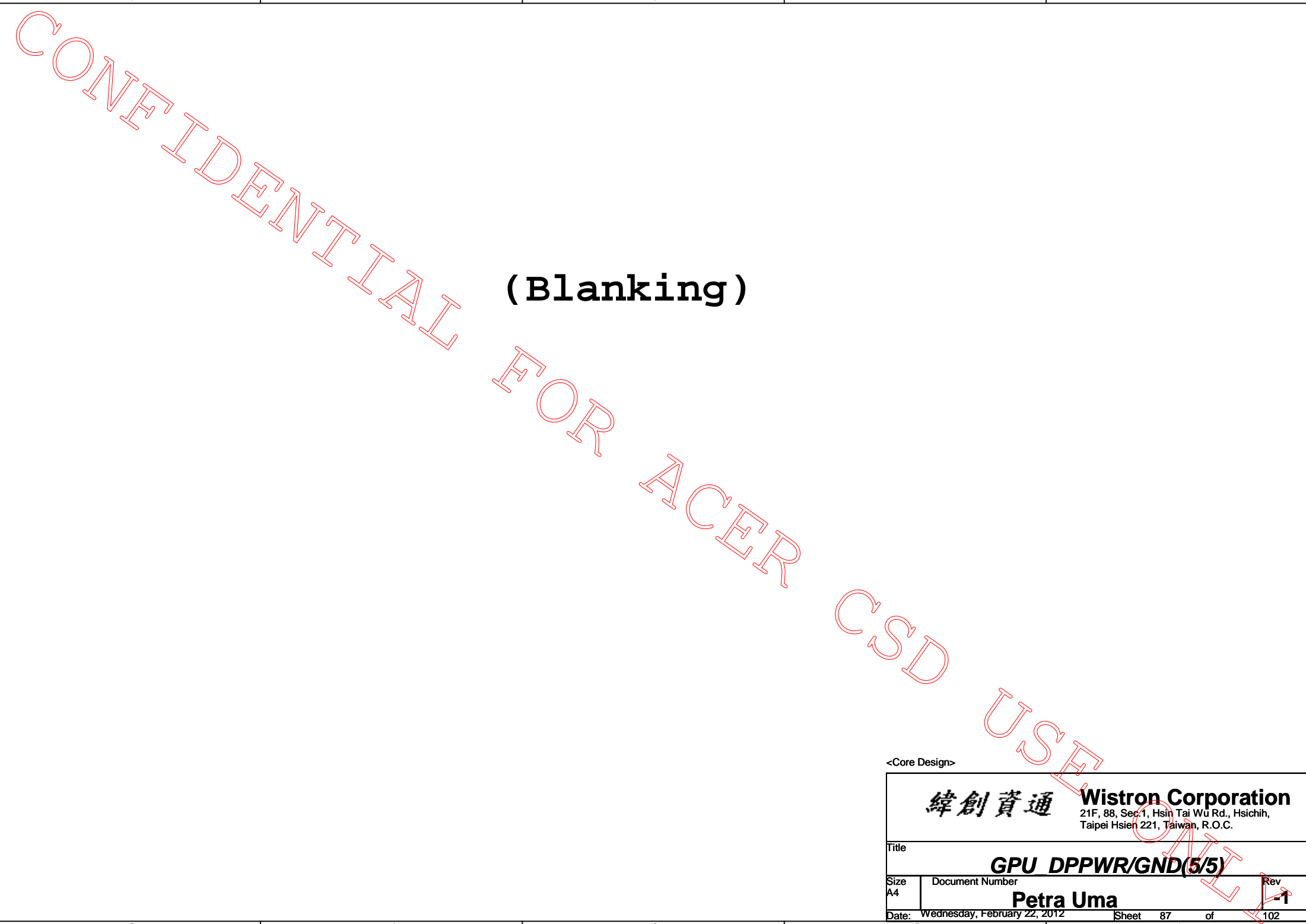


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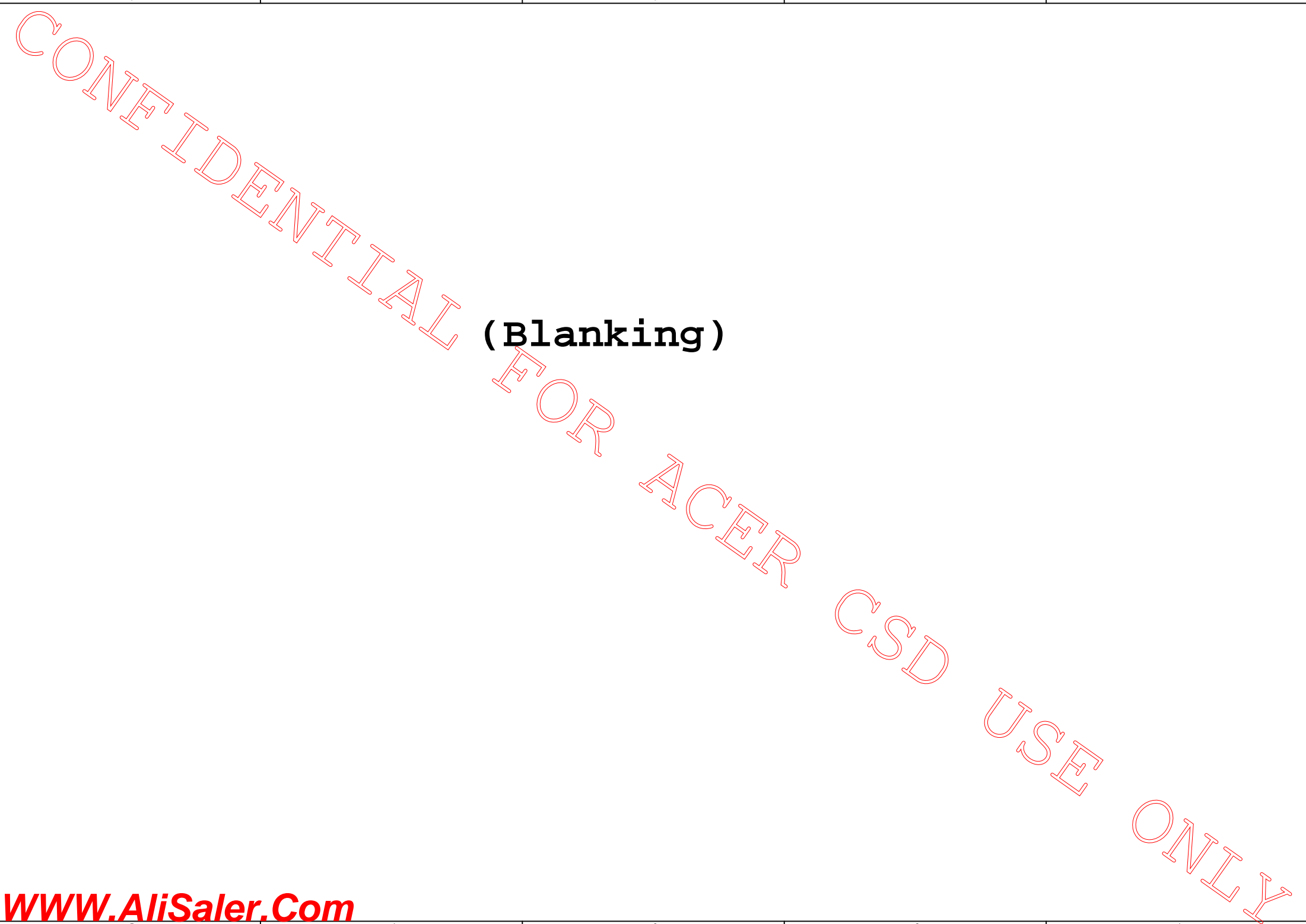
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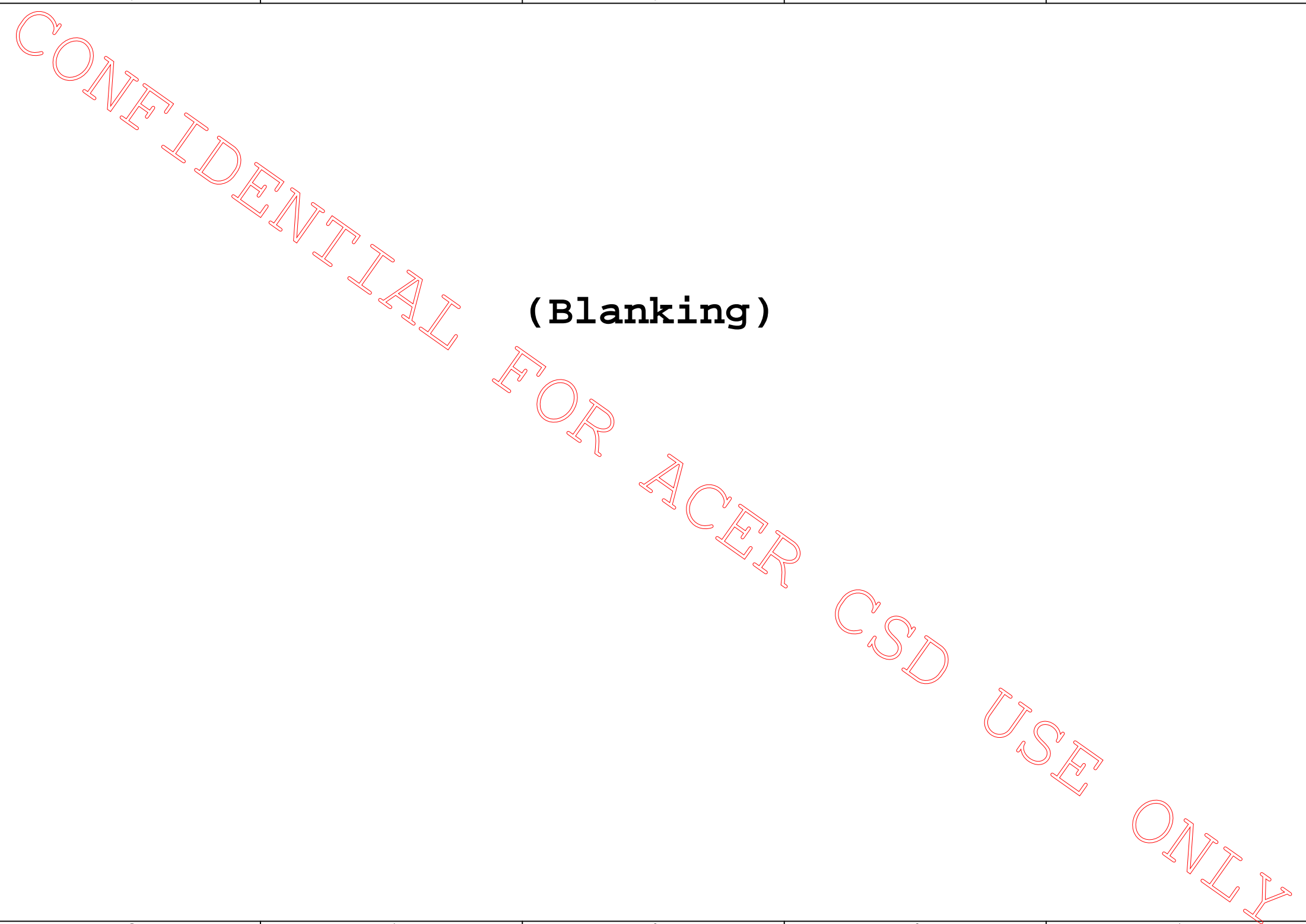
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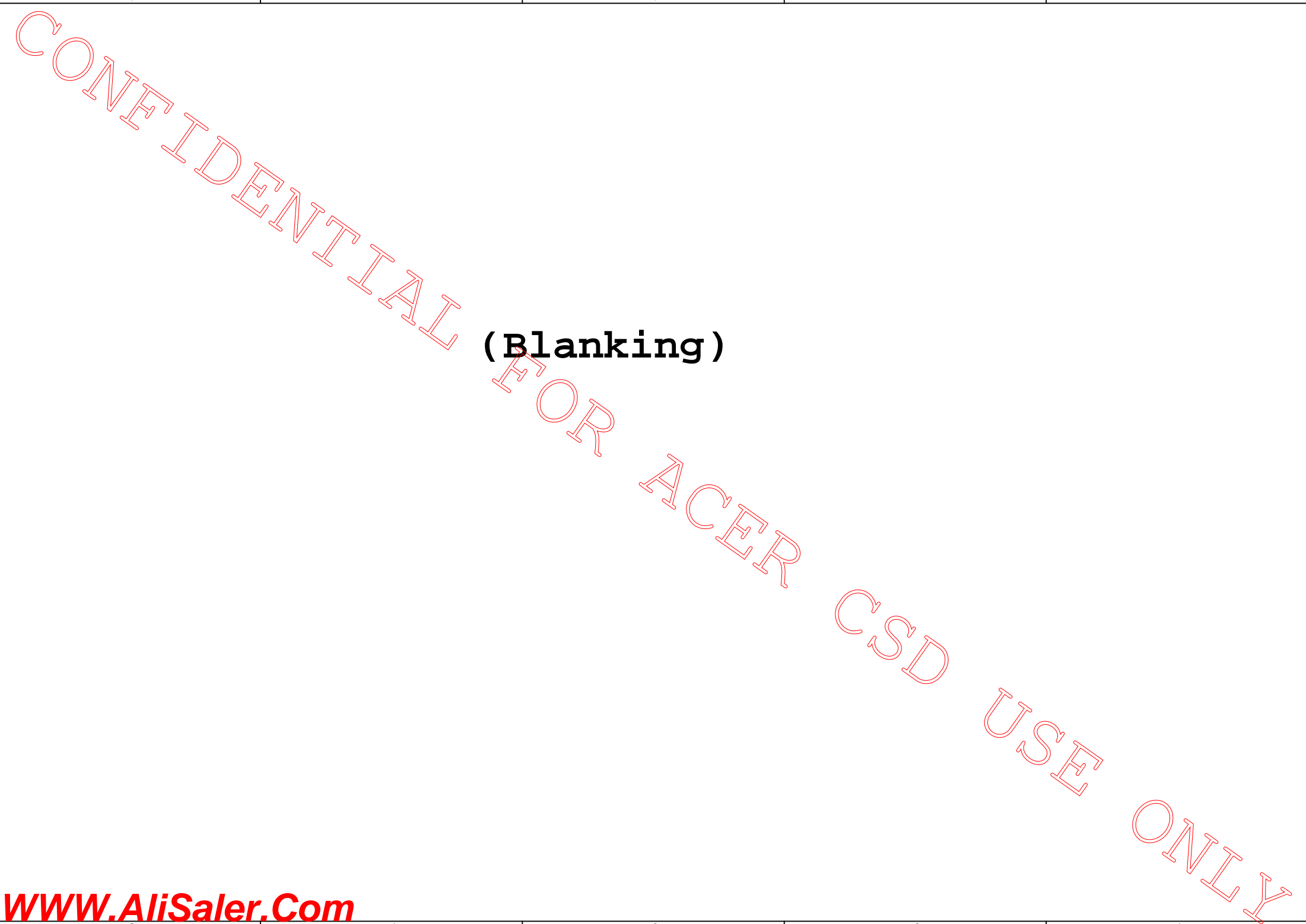
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Title		
GPU DPPWR/GND(5/5)		
Size	Document Number	Rev
A4	Petra Uma	-1
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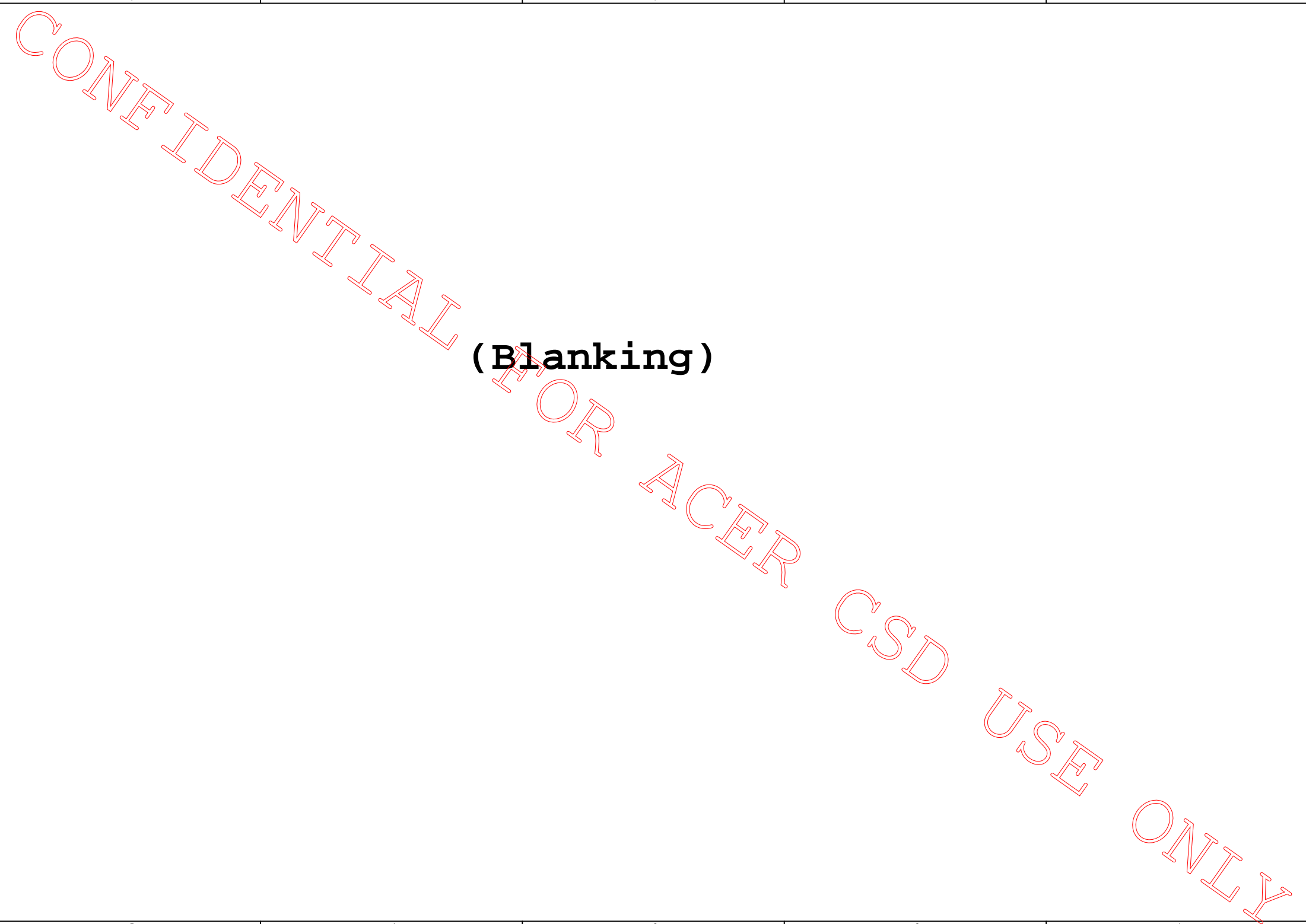
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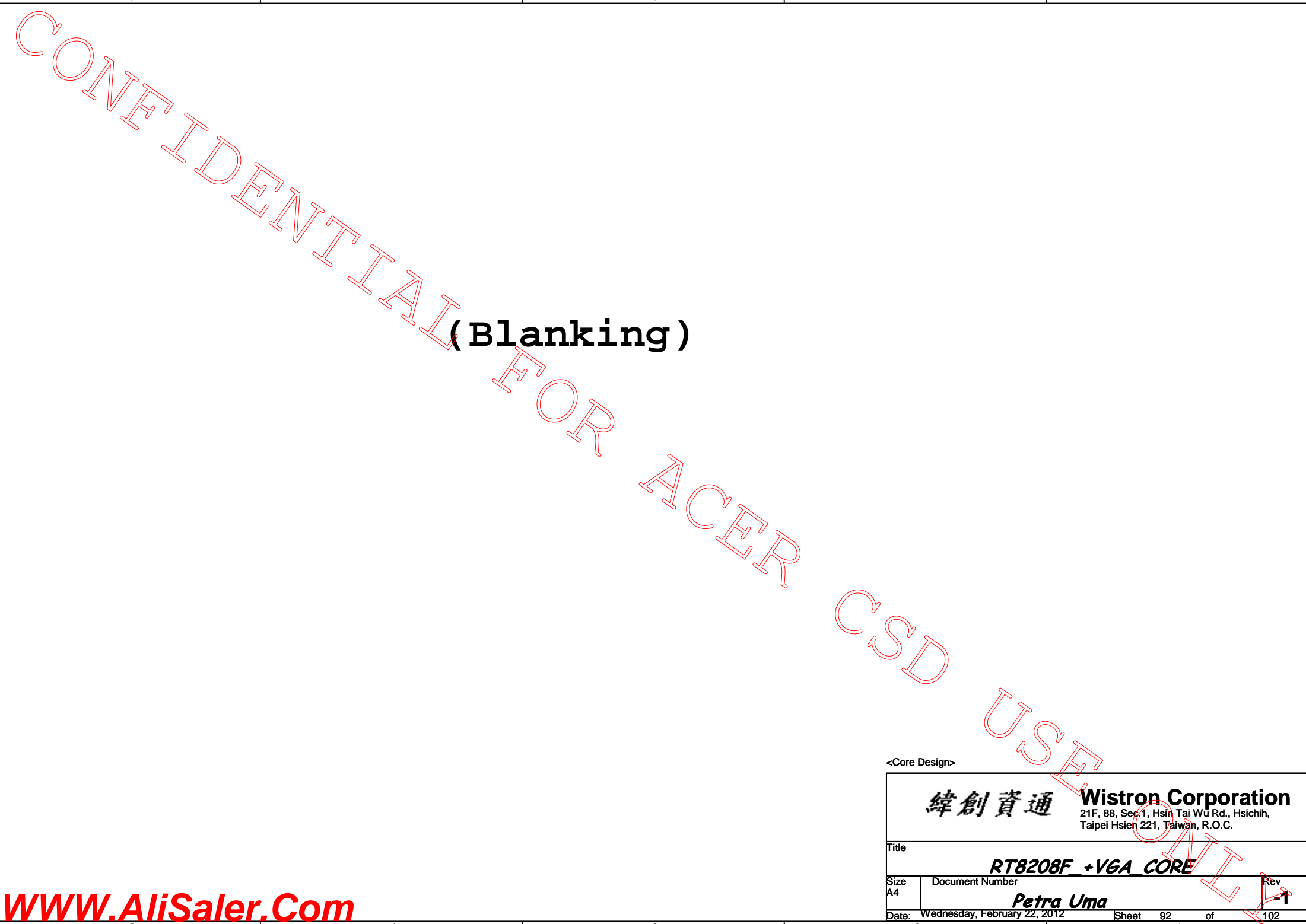
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Title			
RT8208F +VGA CORE			
Size	Document Number		Rev
A4	Petra Uma		-1
Date: Wednesday, February 22, 2012		Sheet 92 of	102

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Title

DISCRETE VGA POWER

Size
A4

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LVDS Channel A

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Panel BL brightness/Power En/BL En

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Title

LVDS Switch

Size

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Title <div>CRT Switch</div>		
Size <div>A4</div>	Document Number <div>Petra Uma</div>	Rev <div>-1</div>
Date: Wednesday, February 22, 2012		Sheet 95 of 103

SSID = SDIO

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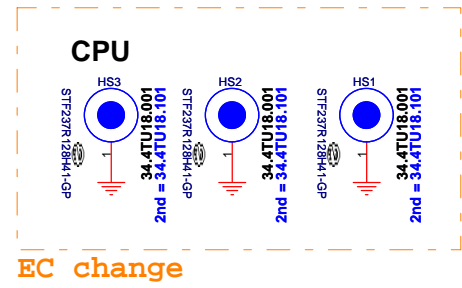
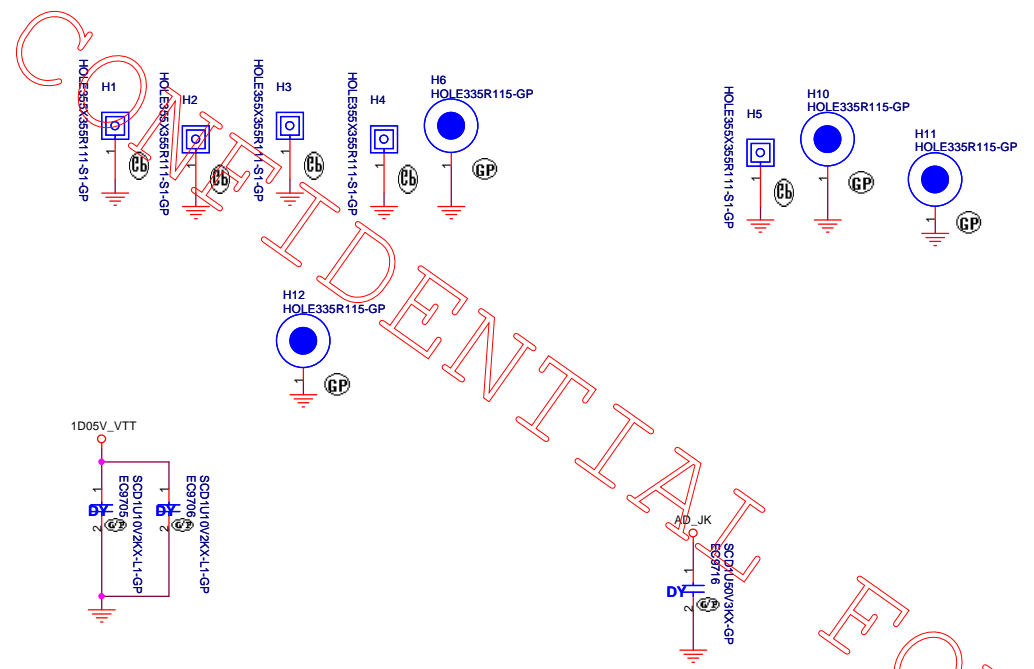
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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title TOUCH PANEL

Size A4 Document Number Petra Uma Rev -1

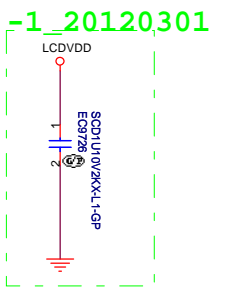
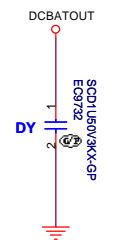
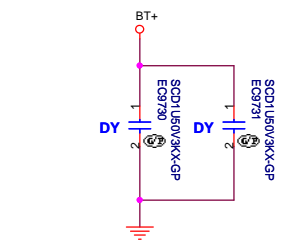
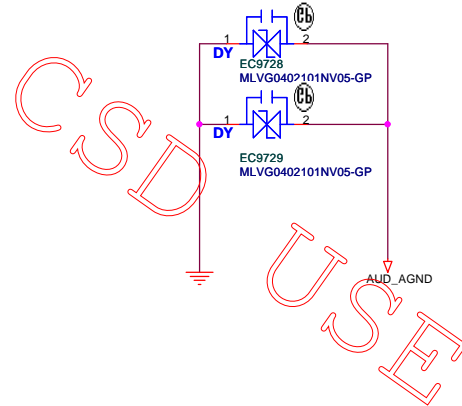
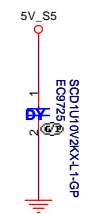
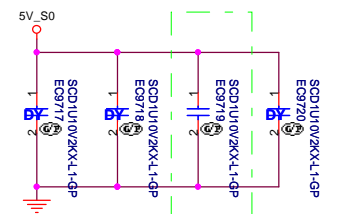
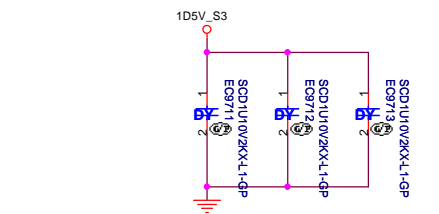
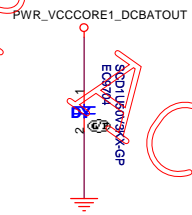
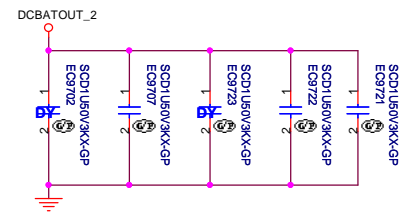
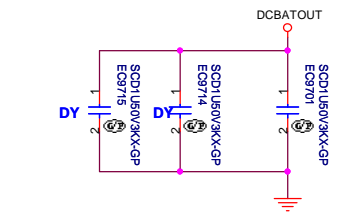
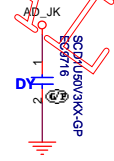
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Check test point

3D3V_S0	1	AFTP1
3D3V_AUX_S5	1	AFTP7
3D3V_S5	1	AFTP8
5V_S5	1	AFTP9
19.27 PM_PWRBTN#	<<<	AFTP10
5.22.36 H_CPUPWRGD	>>>	AFTP11
27.36 S5_ENABLE	<<<	AFTP12
5.18.27.31.36.65.71 PLT_RST#	>>>	AFTP13

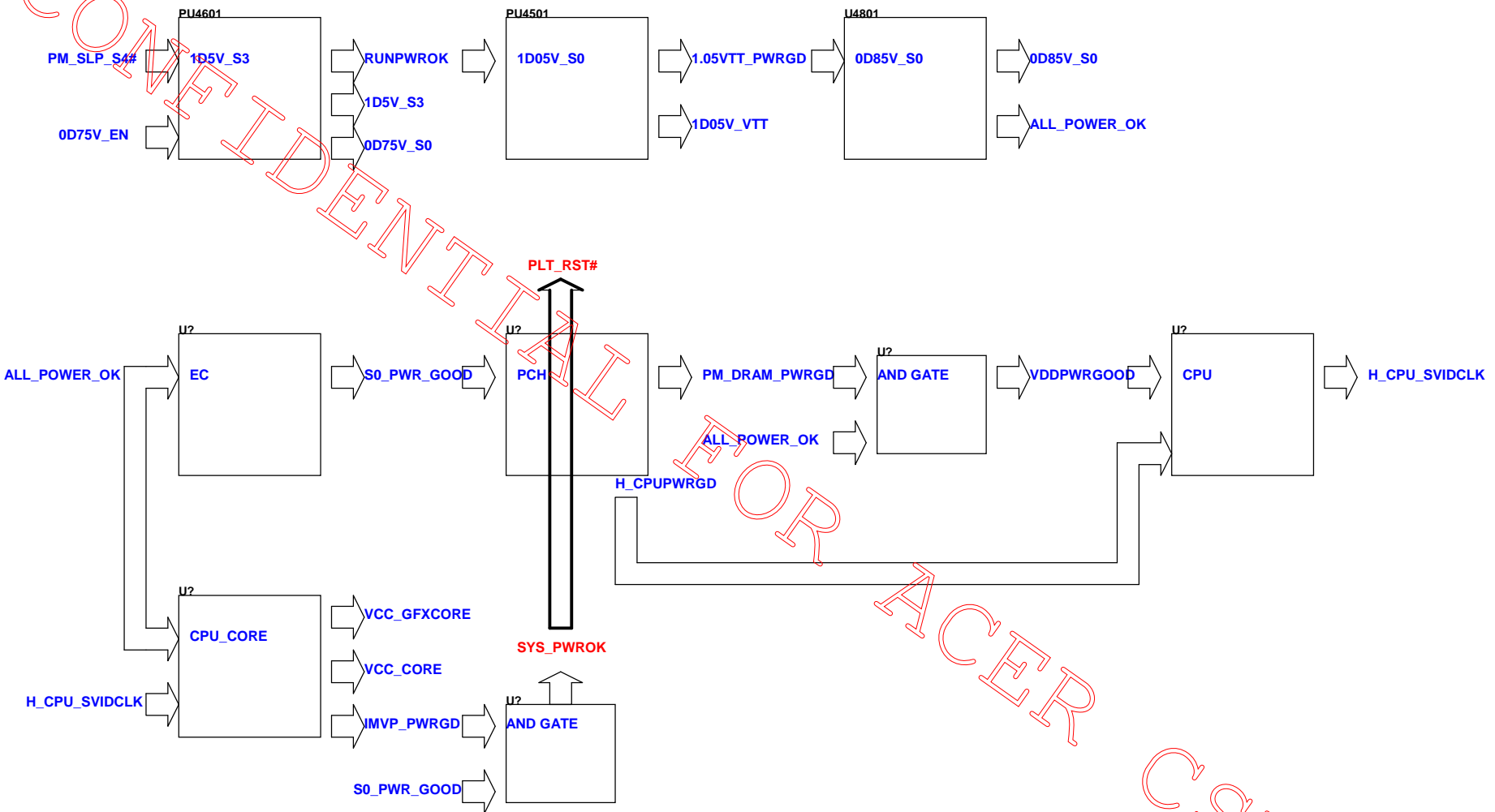
Test Point放在Dimm Door打開可量測處



-1_20120301

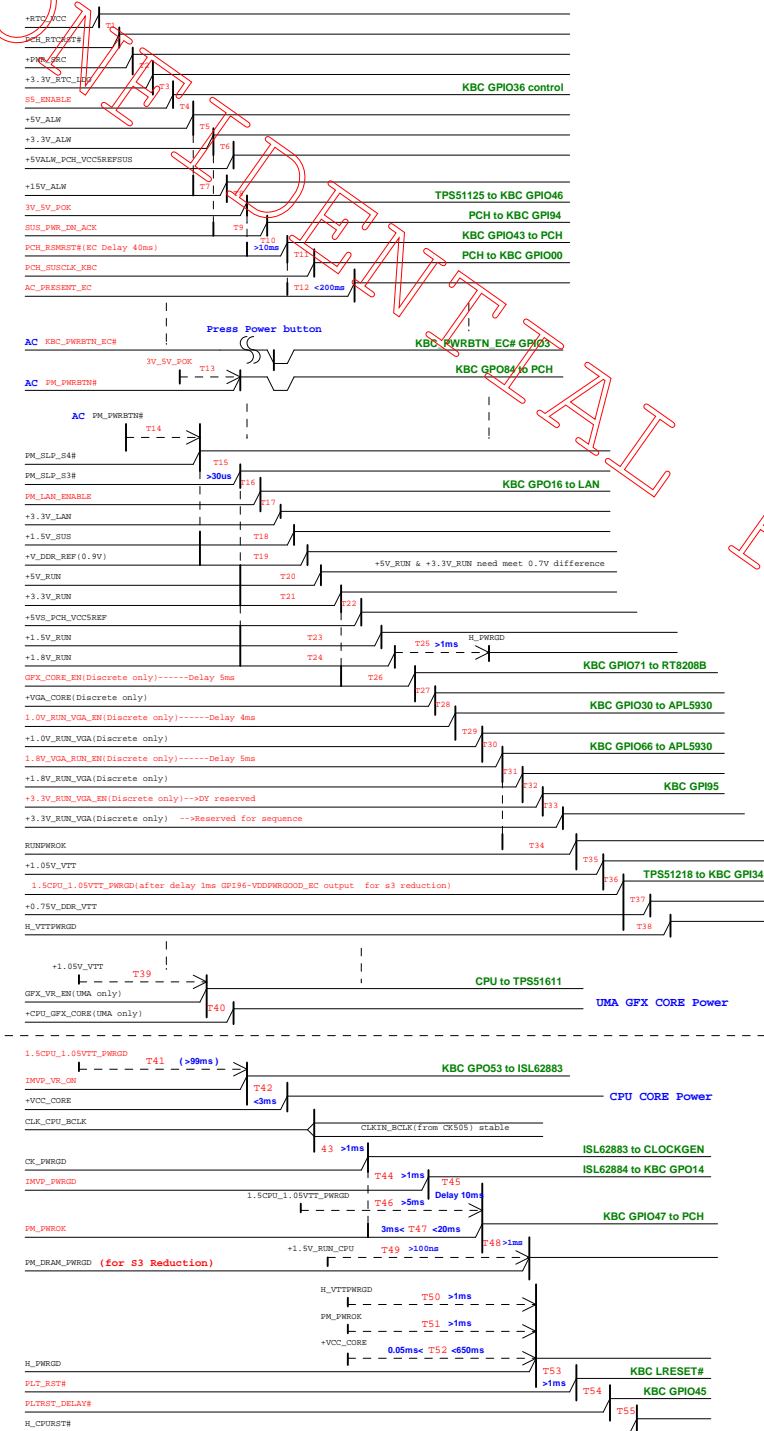
-1_20120301

Power Sequence



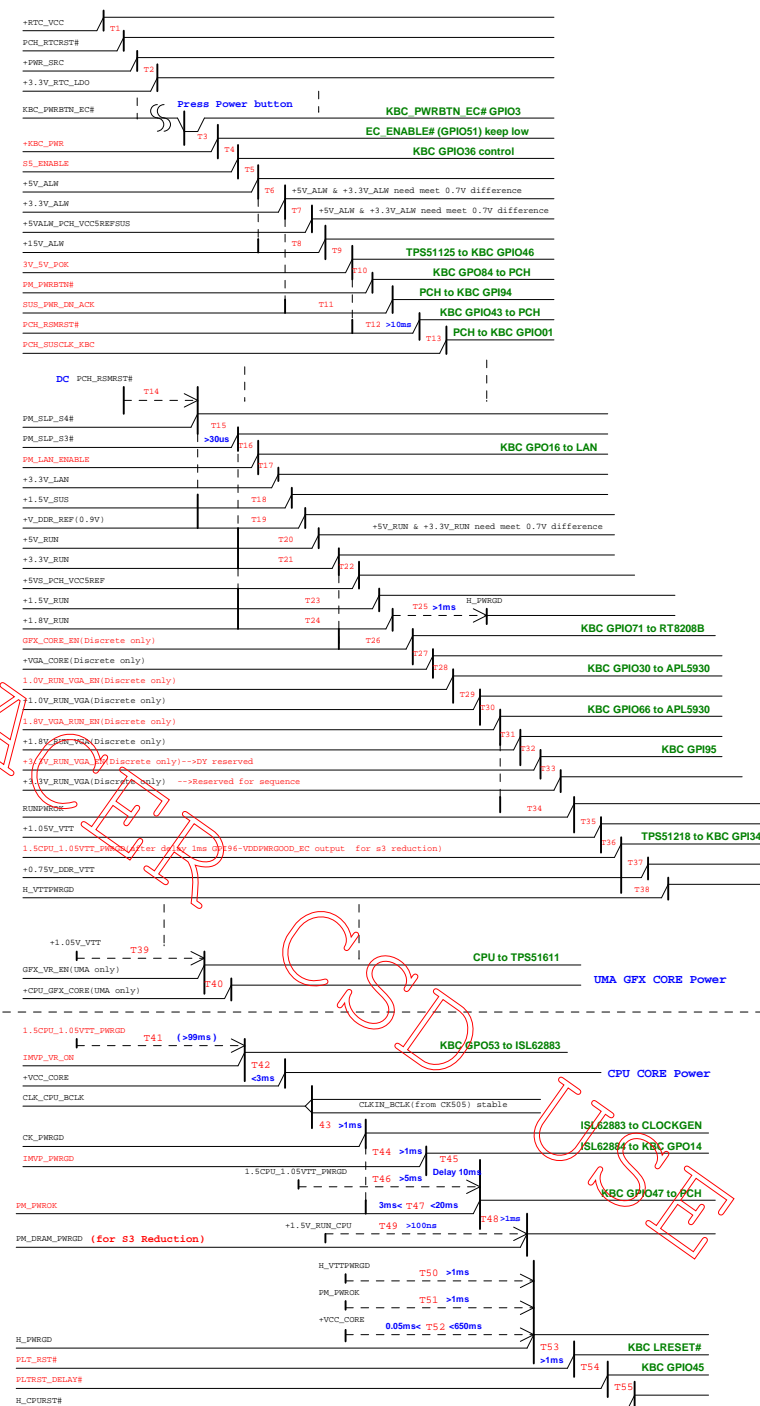
(AC mode)

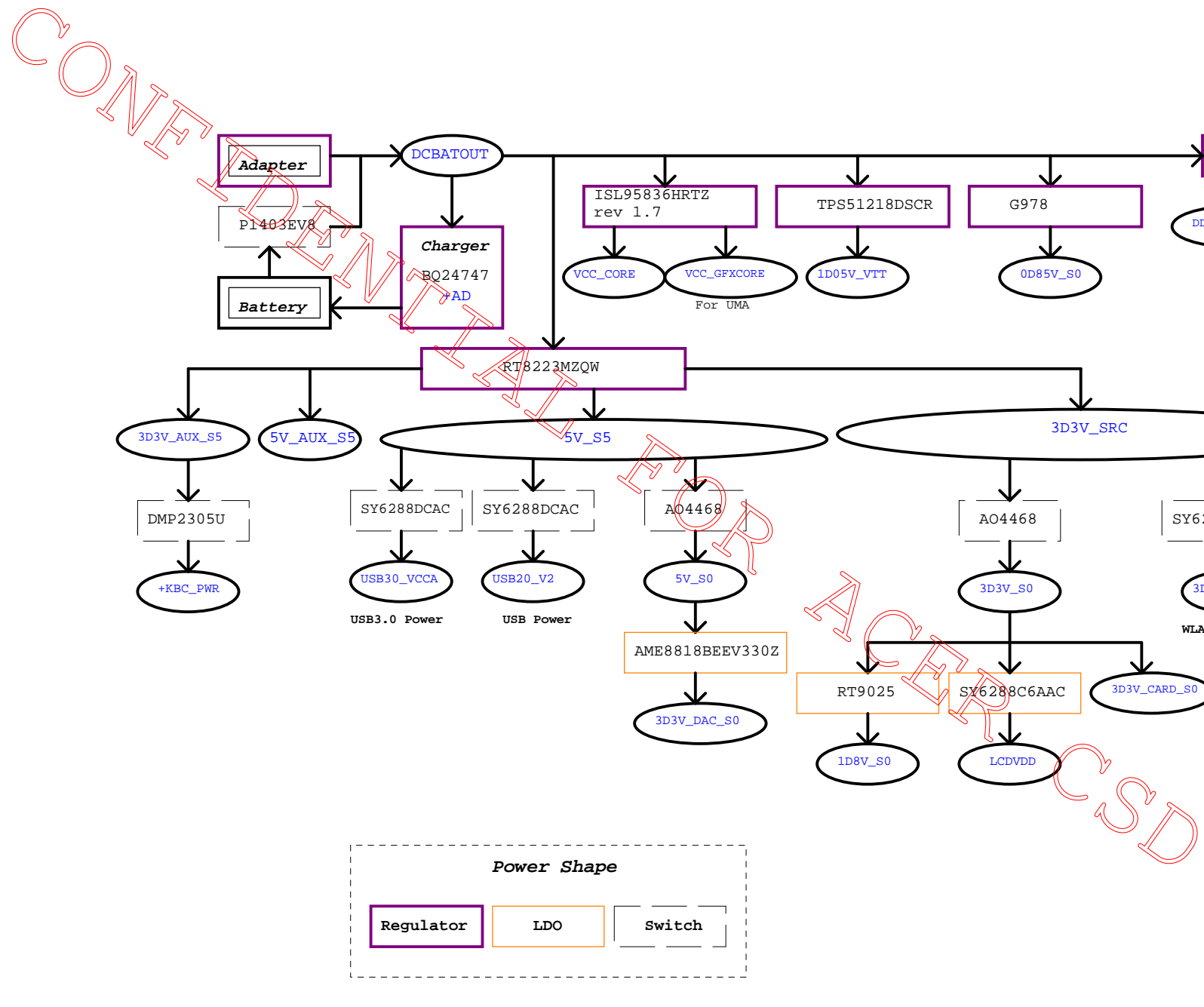
red word: KBC GPIO



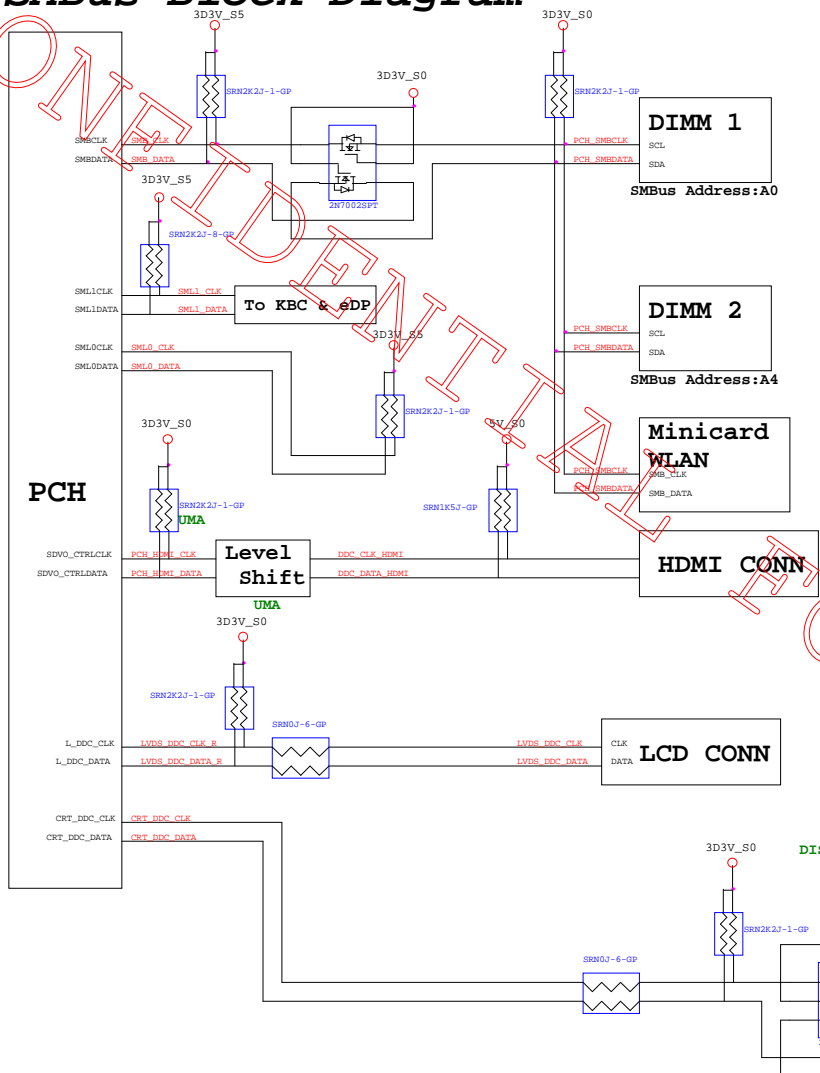
(DC mode)

red word: KBC GPIO

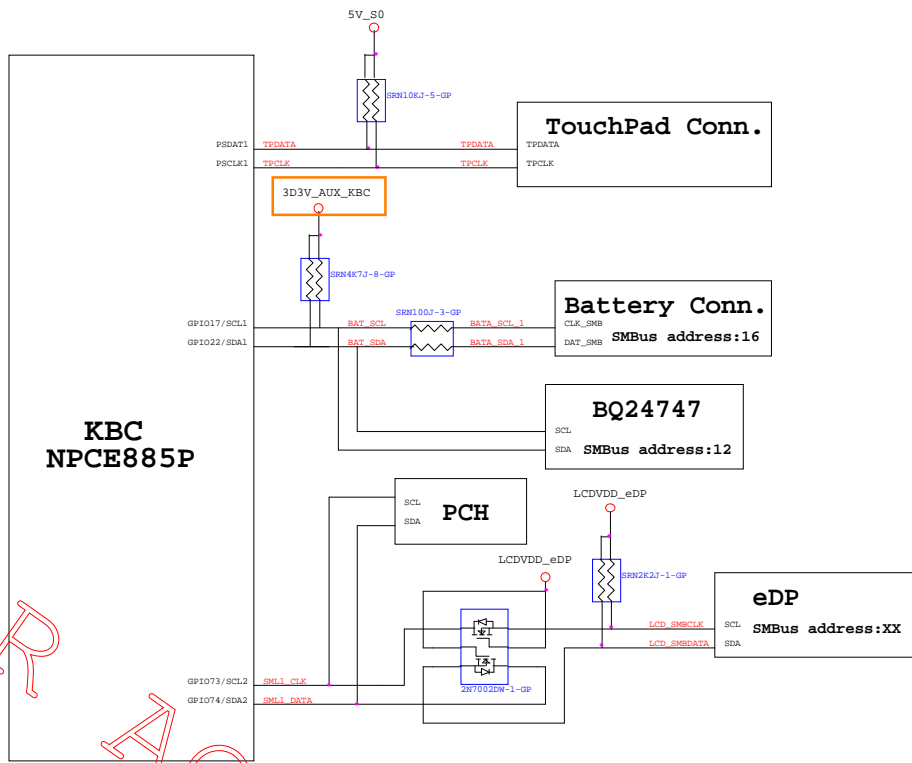




PCH SMBus Block Diagram



KBC SMBus Block Diagram



[illegible]

Thermal Block Diagram

Audio Block Diagram

Thermal NCT7718W

Codec ALC271

SPEAKER

CMBO LOUT

AMIC

PCH SMBUS

2N7002

VR

3V/5V

SC2200P50V2KX-2GP

MMBT3904-3-GP

MMBT3904-3-GP

T8

PAGE28

DXP

P2800_DXP

DXN

P2800_DYN

SML1_CLK

SML1_DATA

THERM_SYS_SHDN#

PURE_HW_SHUTDOWN#

IMVP_PWRGD

PGOD

EN

Put under CPU(T8 HW shutdown)

Place near CPU PWM CORE

Wistron Corporation

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Thermal/Audio Block Diagram

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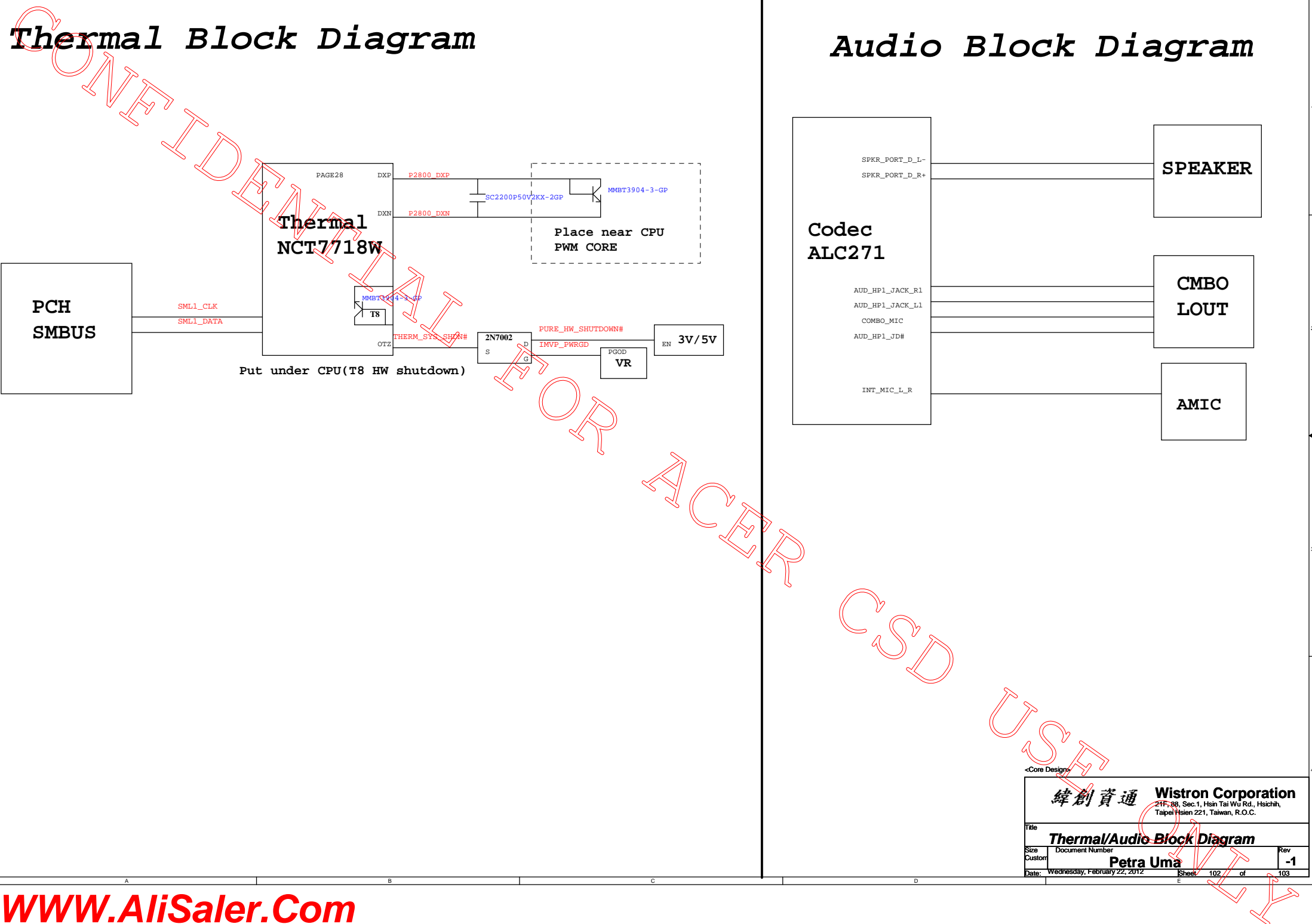
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USE

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(Blanking)

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB charger

Size
A4

Document Number

Petra Uma

Rev
-1

Date: Wednesday, February 22, 2012

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